



# **Final Design Review:**

## ***SNS Normal Conducting Linac***

## ***RF Control System***

Amy Regan

RF Controls Team:

Irene DeBaca, Sung-il Kwon, Roy Lopez, Mark Prokop,  
Tony Rohlev, Dave Thomson, Yi-Ming Wang

**January 16, 2001**

# Agenda

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1. Top Level SNS Linac RF Controls Specification (Regan)
2. Review of PDR Issues (Regan)
3. Manufacturing plan (Regan)
4. Modeling and simulation (Kwon) 30 min

## **Module Design Status – Drawing review, Simulations, Analyses, etc.**

5. FRCM Mother Board & PLDs (Prokop)

20 min

## **WORKING LUNCH**

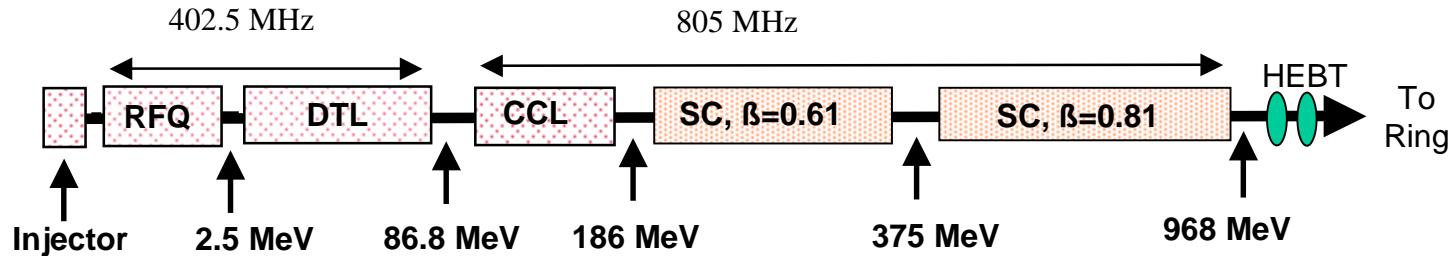
6. RF/Analog Daughter Board (Rohlev) 30 min
7. DSP Daughter Boards (Wang) 20 min
8. HPRF Protect System (Thomson) 30 min
9. Clock Distribution (Regan) 20 min
10. Global Controls Approach (Kerstiens) 15 min
11. Cost and Schedule (Regan) 20 min
12. Remaining Issues (Regan)

# Charge to the Committee



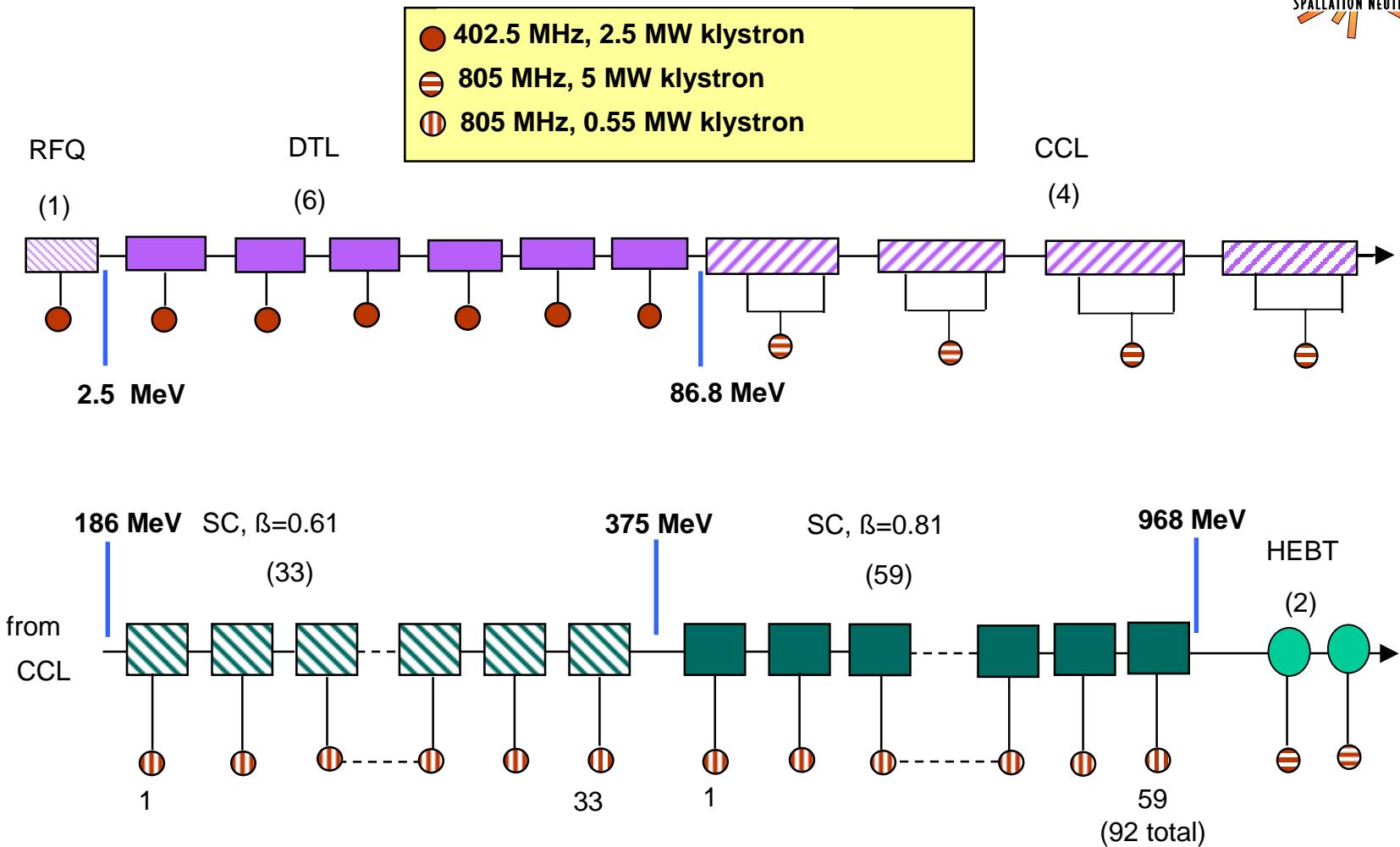
- Is the design sound and will it work?
- Is it consistent with the PDR and its outcome?
- Once the first prototypes prove out, are we ready to proceed with fabrication? (Is engineering approach adequate, yet not overkill?)
- Are interfaces within the RF Control System, as well as external systems, identified?

# NC/SC Linac for SNS

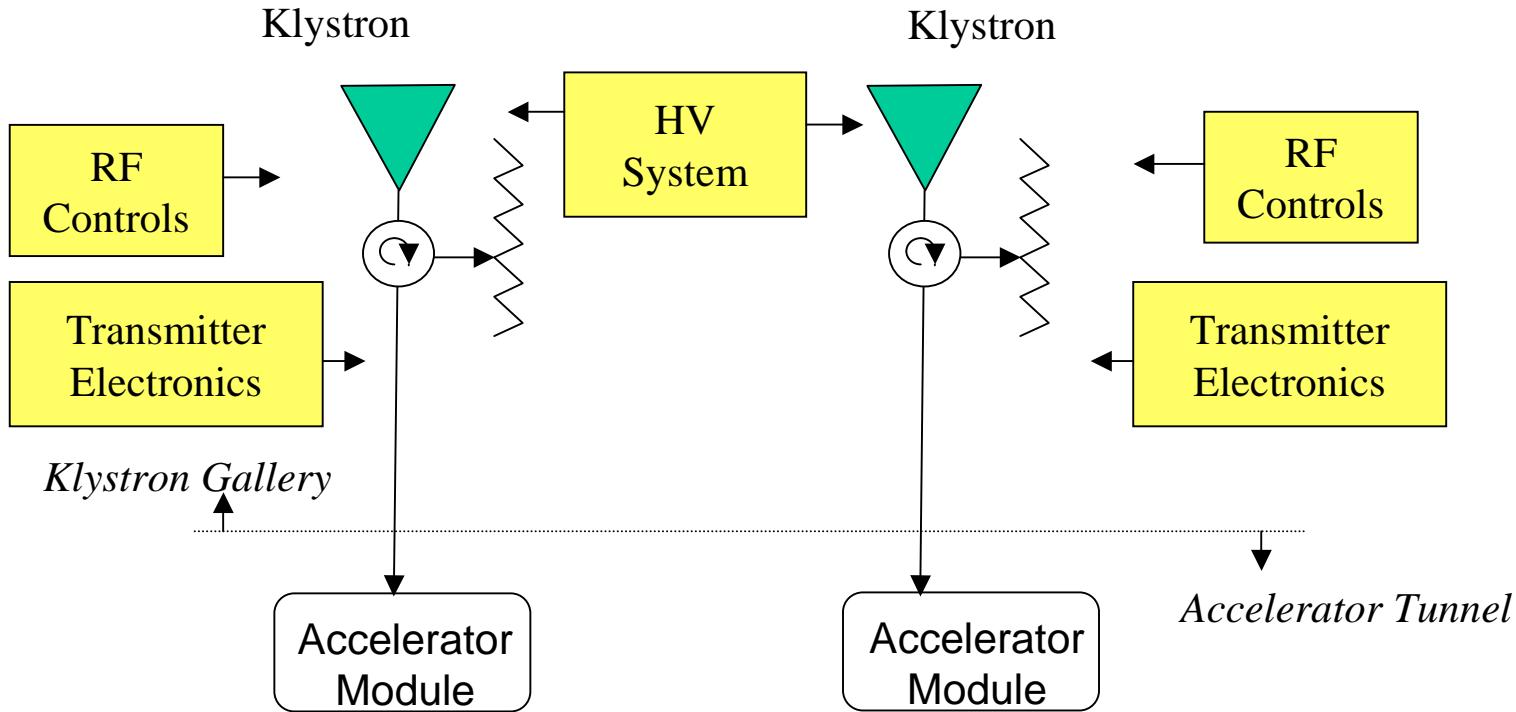


H- energy	968 MeV
Beam power	2 MW, avg.
Pulse Width	1.04 ms
Rep Rate	60 Hz
Klystrons	
402.5 MHz, 2.5 MW pk (iincludes 1 for RFQ, 6 for DTL)	7
805 MHz, 5 MW pk (iincludes 4 for CCL, 2 for HEBT)	6
805 MHz, 0.55 MW pk, SC	92
HV Converter/Modulator Systems	1 for each 5 MW klystron or pair of 2.5 MW klystrons except 1 for RFQ and first 2 DTL tanks and 1 for 2 HEBT cavities 1 for 11 or 12 each 0.55 MW klystrons (16 total, plus 2 for test stands)

# Layout of Linac RF with NC and SC Modules

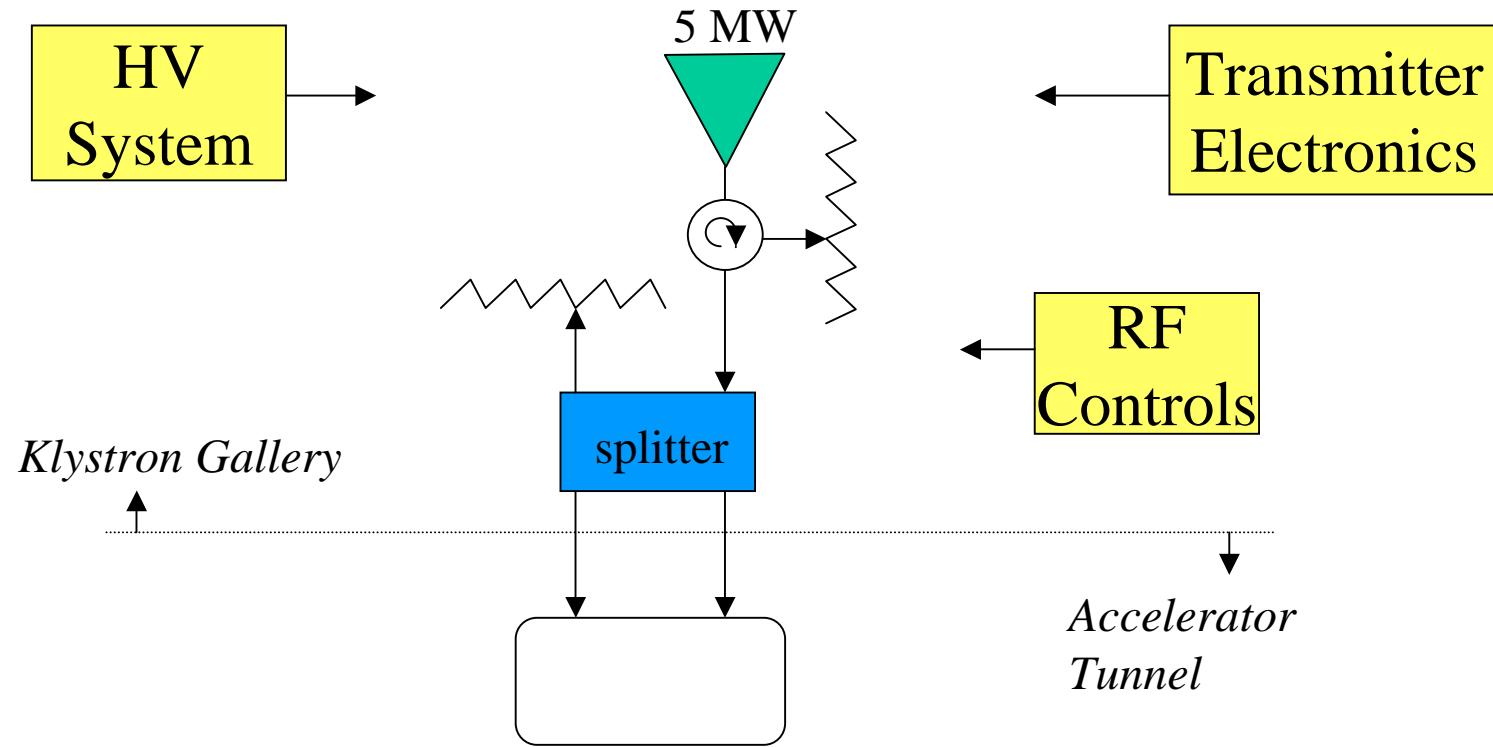


# RF System Block Diagram, 2.5 MW klystrons, 402.5 MHz

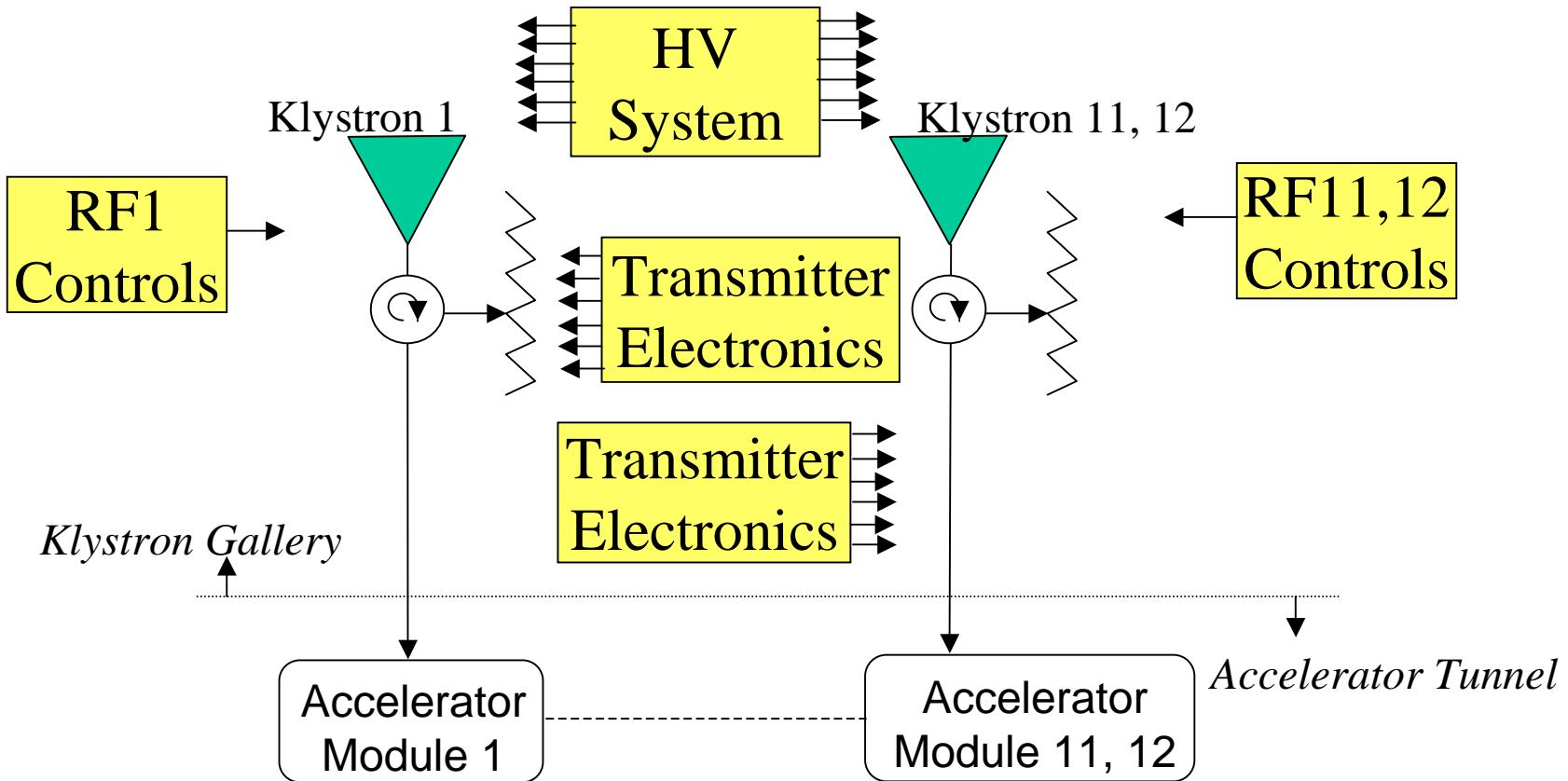


*Note: The RFQ and the first 2 DTL tanks operate from one HV system*

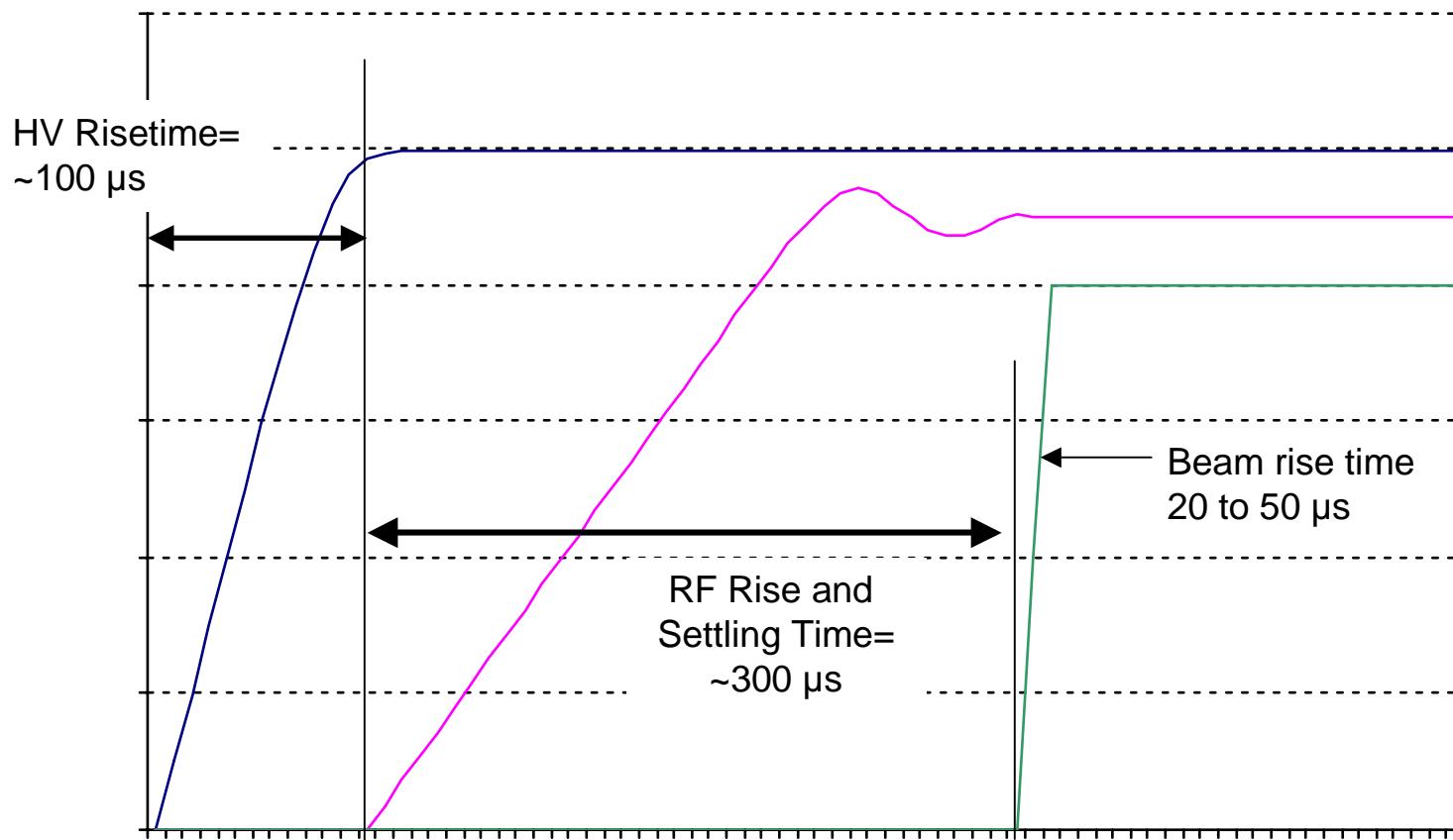
# CCL RF Systems, 5 MW klystrons, 805 MHz



# RF System Block Diagram, 0.55 MW klystrons, 805 MHz (SRF cavities)



# Risetimes and Settling Times



# RF control system requirements drive design



## REQUIRED FUNCTIONS

- Cavity Field Control
- Cavity Resonance Control
- RF Reference generation and distribution
- HPRF protection

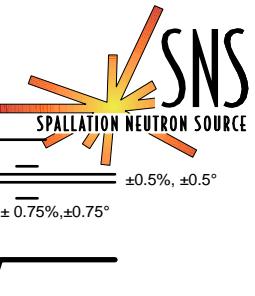
## NC SYSTEM CONFIGURATIONS

- Single 2.5 MW klystron driving single cavity (402.5 MHz)
- Single 5 MW klystron driving single cavity through a split (805 MHz)
- SC: 550 kW klystrons driving single cavities

## ANTICIPATED OPERATIONAL & CONDITIONING SCENARIOS

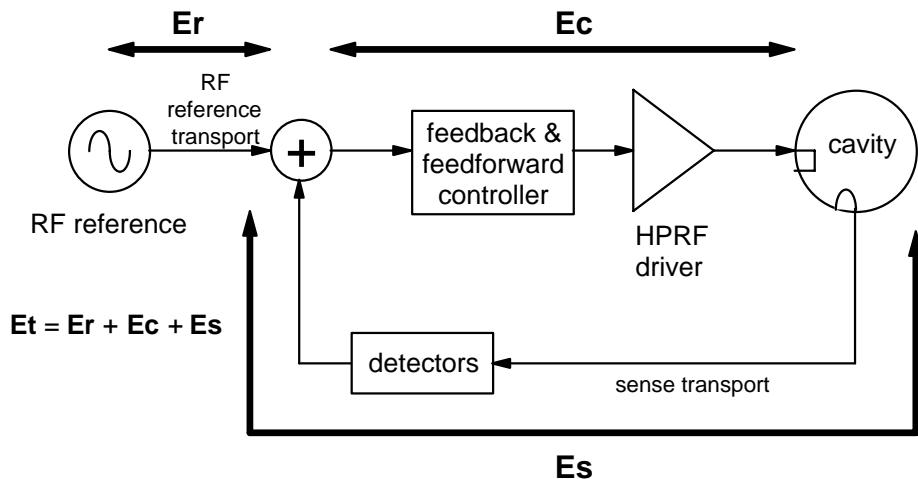
- Pulsed beam, Pulsed RF
- 60 Hz rep rate
- 68% chopping, 36 mA avg

# RF Control System Requirements



<b>FIELD CONTROL</b> $\pm 0.5\%$ amplitude, $\pm 0.5^\circ$ phase	per cavity  <p>A diagram showing a single RF signal waveform. The waveform consists of a series of sharp, narrow pulses. The baseline is dashed, and the signal is solid. The first pulse is positive, followed by a negative pulse, then another positive pulse, and so on. The text "per cavity" is positioned to the left of the waveform.</p>	 <p>A diagram showing two RF signal waveforms side-by-side. Both waveforms show a sequence of pulses. The top waveform has a larger amplitude than the bottom one. The text "± 0.5%, ± 0.5°" is above the top waveform, and "± 0.75%, ± 0.75°" is below the bottom waveform.</p>
<b>RESONANCE CONTROL</b> Maintain cavity resonance	<u><b>NC</b></u> 402.5 MHz: RFQ $f_0 \pm 15$ kHz $(Q_L = 3300)$ $BW = 122$ kHz	<u><b>SRF</b></u>
	402.5 MHz: DTL $f_0 \pm 2$ kHz $(Q_L = 25,000)$ $BW = 16$ kHz	805 MHz: med. $\beta$ $f_0 \pm 500$ Hz $(Q_L = 733,000)$ $BW = 1$ kHz
	805 MHz: CCL $f_0 \pm 10$ kHz $(Q_L = 10,000)$ <small>(smallest bandwidth case)</small> $BW = 80$ kHz	805 MHz: high $\beta$ $f_0 \pm 500$ Hz $(Q_L = 699,000)$ $BW = 1.1$ kHz

# Error Allocation



$Er$  = reference line transport error

$Ec$  = residual control loop error

$Es$  = sense line and detection error

$E_t$  = total system error

## PERFORMANCE OBJECTIVES

PEAK AMPLITUDE ERROR:  $\leq 0.5\%$

PEAK PHASE ERROR:  $\leq 0.5^\circ$

## TOLERANCE BUDGET

	-AMPLITUDE (%)	PHASE
$Er$	N/A	$\pm 0.15$
$Es$	$\pm 0.2$	$\pm 0.15$
$Ec$	$\pm 0.3$	$\pm 0.2$

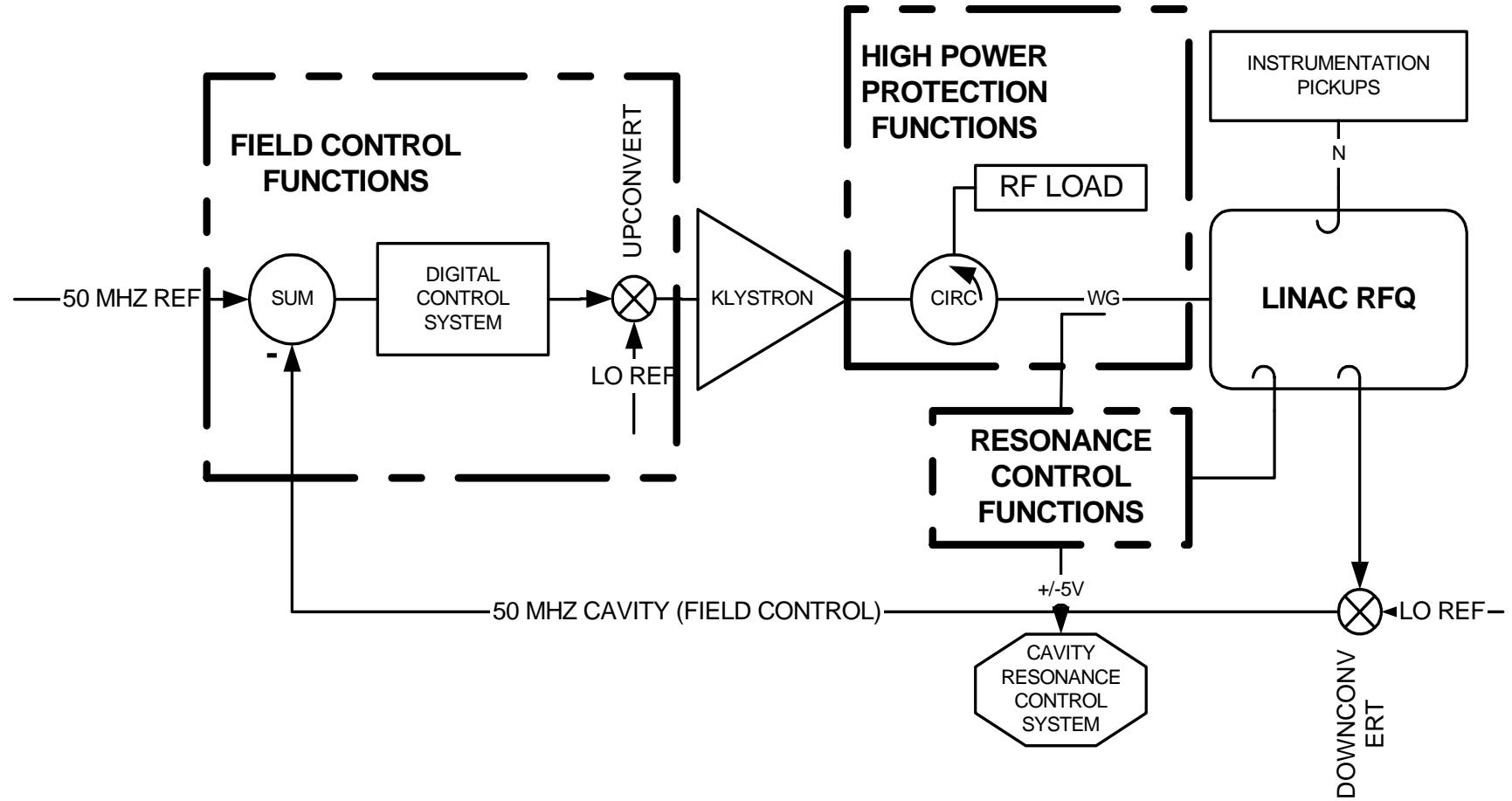
# PDR ISSUES & RESOLUTION

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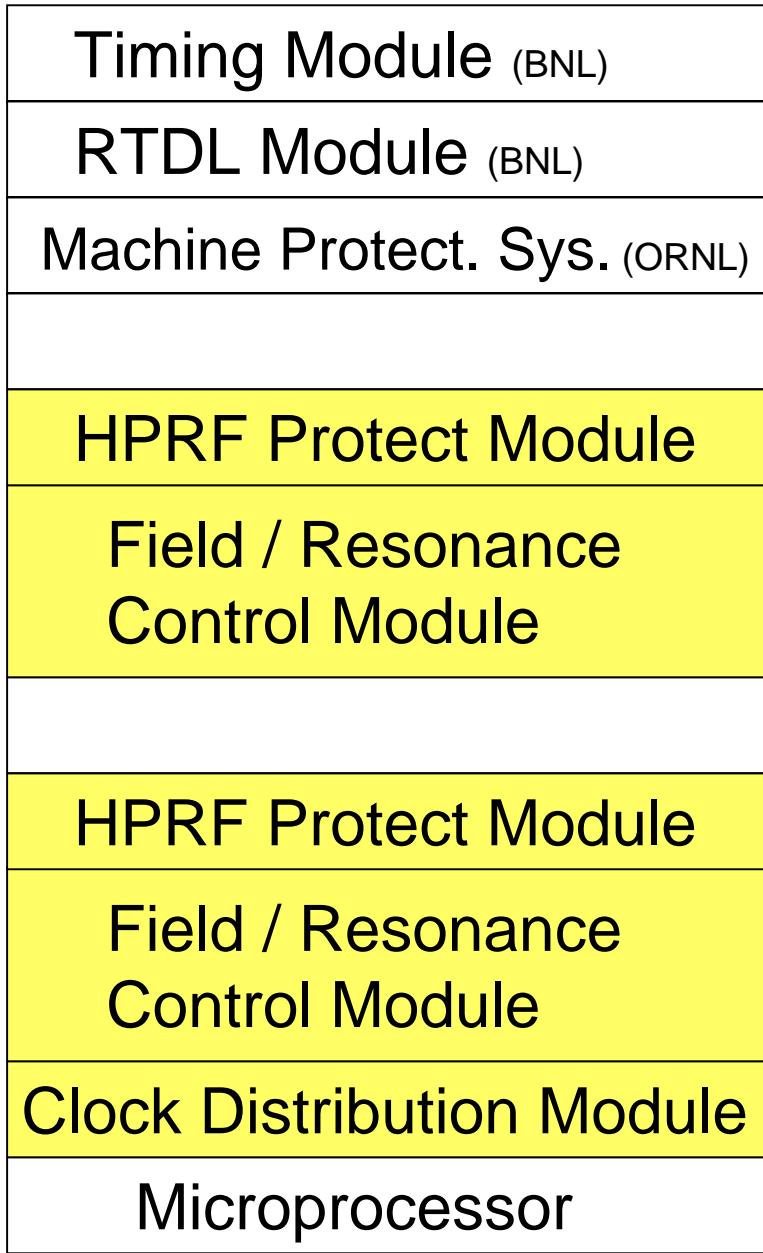
- NEED GOOD SYSTEMS ENGINEERING
  - We're working on it. Video Conferencing, publication of RF System Description, RF System Design Criteria Document, Modeling-based issues brought up,...
- AGGRESSIVE DEVELOPMENT SCHEDULE - FREEZE DESIGN
  - Hardware I/O still an issue, but internal firmware scheme will help
  - Video Conferencing helps, but still a disconnect exists between labs
- HIGH BUDGET
  - Not really. Based on labor rates, vendor quotes, hands-on experience, etc.
- DEVELOPMENT RISK FOR “NEAT” FEATURES
  - We've eliminated them wherever possible. A few requests from top level ORNL personnel still necessitate a couple of bells & whistles
    - (e.g. Dave's spare FOARC binary inputs; accommodate 8 modes)
- SRF BEING IGNORED?

# RFCS Functional Block Diagram



# SRF RF Control System Architecture

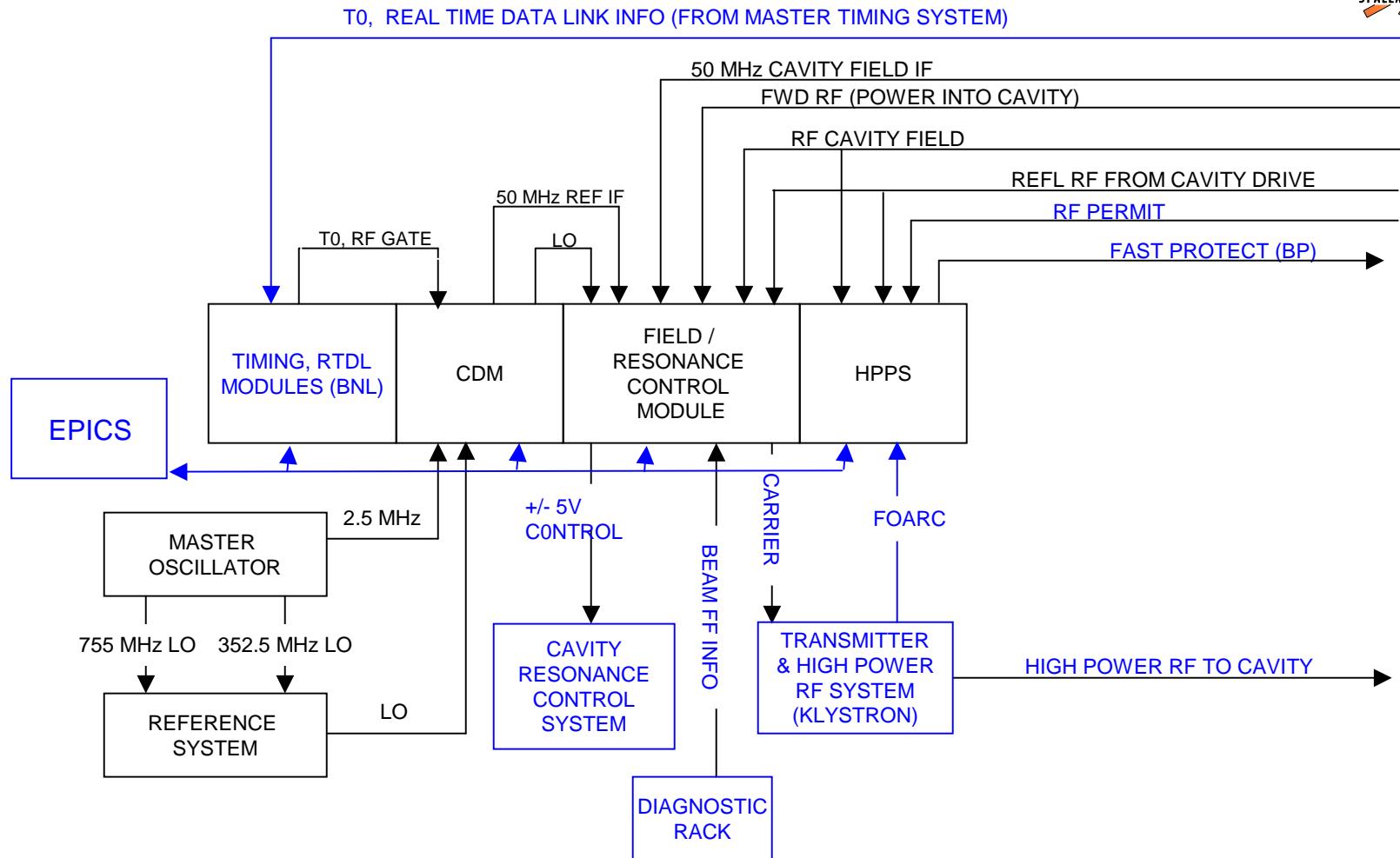
## 2 systems / VXIbus crate



■ LANL-designed VXIbus module

Machine Protection System, Timing System, Real Time Data Link Interface Modules still to be defined

**RFCS interfaces with a variety of external systems.**  
 This implies much more involvement of RFCS personnel over other RF people during beam startup.



# VXbus Module Manufacturing Details

NC: 1 RFQ, 6 DTL, 4 CCL, 2 HEBT, 1 test stand, 2 spare  $\Rightarrow$  3 modules/sys.

SRF: 92 (81) cavities, 1 test stand, 6 spares  $\Rightarrow$  2.6 modules/system

} 303 modules  
(275)



## Initial Fabrication & Testing RF Control System

Prototype Designs & Fabrication at LANL

Complete documentation for external manufacture and test

## CONTRACT MANUFACTURER SELECTION

### Specifications

100% Inspection

IPC 610 CLASS 3

### Capabilities Required

Surface Mount Technologies

Ball Grid Array Application & Inspection with x-ray camera

Purchasing Components / Kitting

Cable Assemblies

Full Functional Testing

### Resources (Albuquerque)

Sparton L & L

Delta Group MPC Technologies

# VXIbus Module Testing Details



Module Manufacturer will perform Bed of Nails test (continuity, voltages, etc.)

Same, or other, Contract Manufacturers with RF/Digital Testing capabilities exist in Albuquerque. (as we select vendor for PCB manufacture we will weigh their ability to perform follow-on full-functional testing as well. More efficient than going to different test vendor).

Our plan - Have Contract Manufacturer perform full-functional test.

We will provide detailed Test Procedures.

We anticipate LabVIEW interface software will drive various tests (RAM, etc.) .

Tested modules will be shipped directly to ORNL.

Backup plan - we perform testing at LANL, with support from ORNL. However, this is more time-intensive, and not nearly as cost-effective.

# Modeling Work: Matlab is the basis for RF Control System models



- Mathematical formulation for each block using modern control theory
- Analysis and Synthesis : Matlab m-files

Synthesis of all three Required Controllers

PI Feedback Controller

Feedforward Controller - (Robust) Iterative Learning Controller

Gain Scheduling Controller

Noise, Disturbance, Parameter Perturbation Analysis

Field Feedback Loop Uncertainty and Disturbance Analysis

Low Level RF Forward Loop Uncertainty and Disturbance Analysis

Beam Loading Effect Analysis

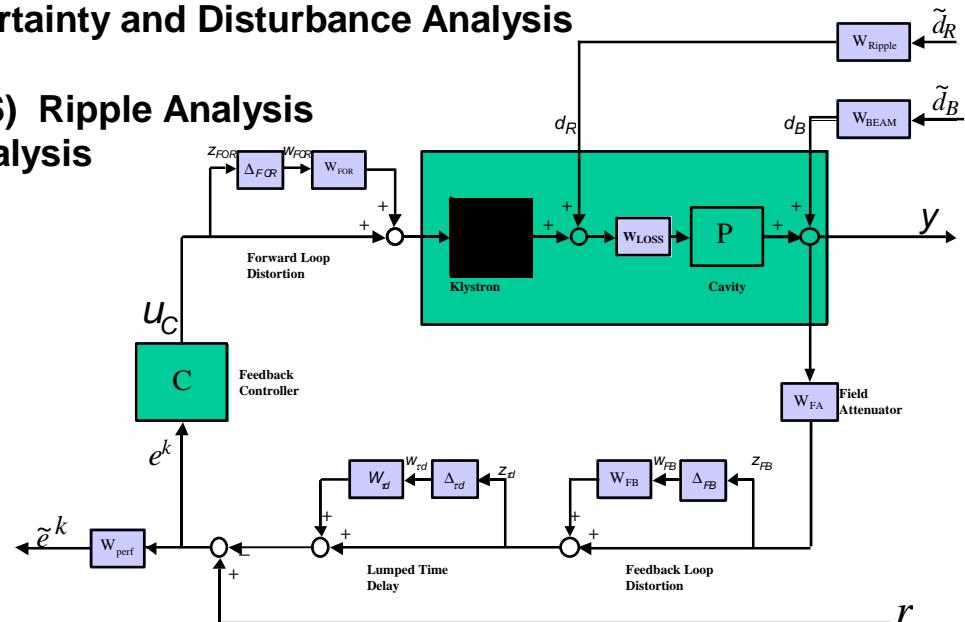
High Voltage Power Supply (HVPS) Ripple Analysis

Cavity Parameter Perturbation Analysis

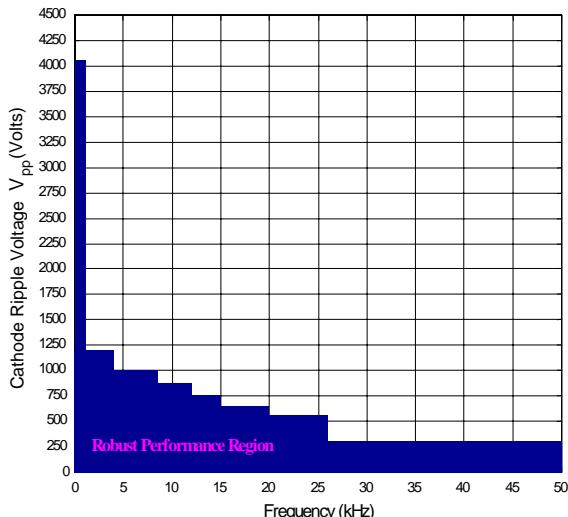
Lorentz Force Detuning

Microphonics

- Simulation and Verification :  
Matlab Simulink Models



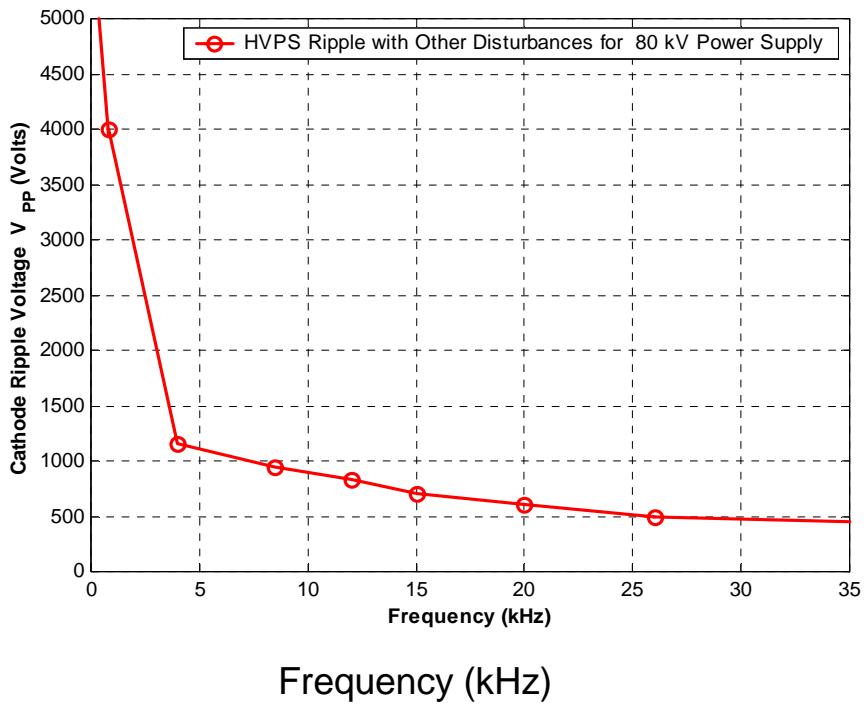
# Modeling has been expanded to help define other parts of the system. e.g. HVPS Ripple Specification



Cathode Ripple $V_{pp}$ (Volts)	Frequency limits for Robust Performance (kHz)
250	Unlimited
500	26.0
600	20.0
700	15.0
825	12.0
950	8.5
1150	4.0
4000	0.8



Cathode Ripple Voltage  $V_{pp}$  (Volts)





# RF Controls FINAL Design Review

## ***SNS Normal Conducting Linac RF System - Control System Modeling***

Sung-il Kwon

January 16, 2001

# Modeling Issues

## Approaches

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- Two Approaches are Considered
  - Nonlinear Simulation Model : Time Domain Model
    - MATLAB/SIMULINK Block Model
    - Time Domain Simulation
    - Nonlinearities in System
    - Disturbances, Noises effects are Verified through Simulation
  - Linearized Uncertainty Model : Frequency/Time Domain Model
    - Enjoy the Frequency Domain System Parameters
      - Open/Closed Loop System Bandwidths
      - Determined Feedback, Feedforward Controller Parameters
    - Analytic Check of Nonlinear Time Domain Simulation
      - Disturbances, Noises effects are Analyzed in Frequency Domain

# Modeling Issues

## System Components

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- Nonlinearities : Klystron
  - Make it difficult to use modern linear system theory for analysis and synthesis
  - Need to be linearized around operating point sacrificing the transient behavior
- Noises, Disturbances, Distortions
  - HVPS ripple
  - Forward Loop Distortions due to RF components
  - Feedback Loop Distortions due to RF components, cable noises
  - Beam Noise : 1.2 % in amplitude, dominant frequency 30 kHz
  - Chopped Beam : 1.05 MHz
  - Higher order modes in passband

# Modeling Issues

## System Components

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- Noises, Disturbances, Distortions
  - Time Delays : High Frequency Uncertainty
    - Klystron due to the electron transient time and response time : 150 nsec
    - Waveguide : 116.5 nsec ----- 100ft
    - Feedback cable : 121.0 nsec ----- 100ft
    - Signal Processing and Controller due to FIR filter, computation time : xxx usec
- Controllers
  - Transient :  $\pm 0.75\%$  Amplitude Error  
 $\pm 0.75\text{ Deg}$  Phase Error
  - Steady State:  $\pm 0.5\%$  Amplitude Error  
 $\pm 0.5\text{ Deg}$  Phase Error
  - Feedback Controller : PI Controller
  - Feedforward Controller : Iterative Learning Controller

# Modeling Issues

## Parameters to be Determined

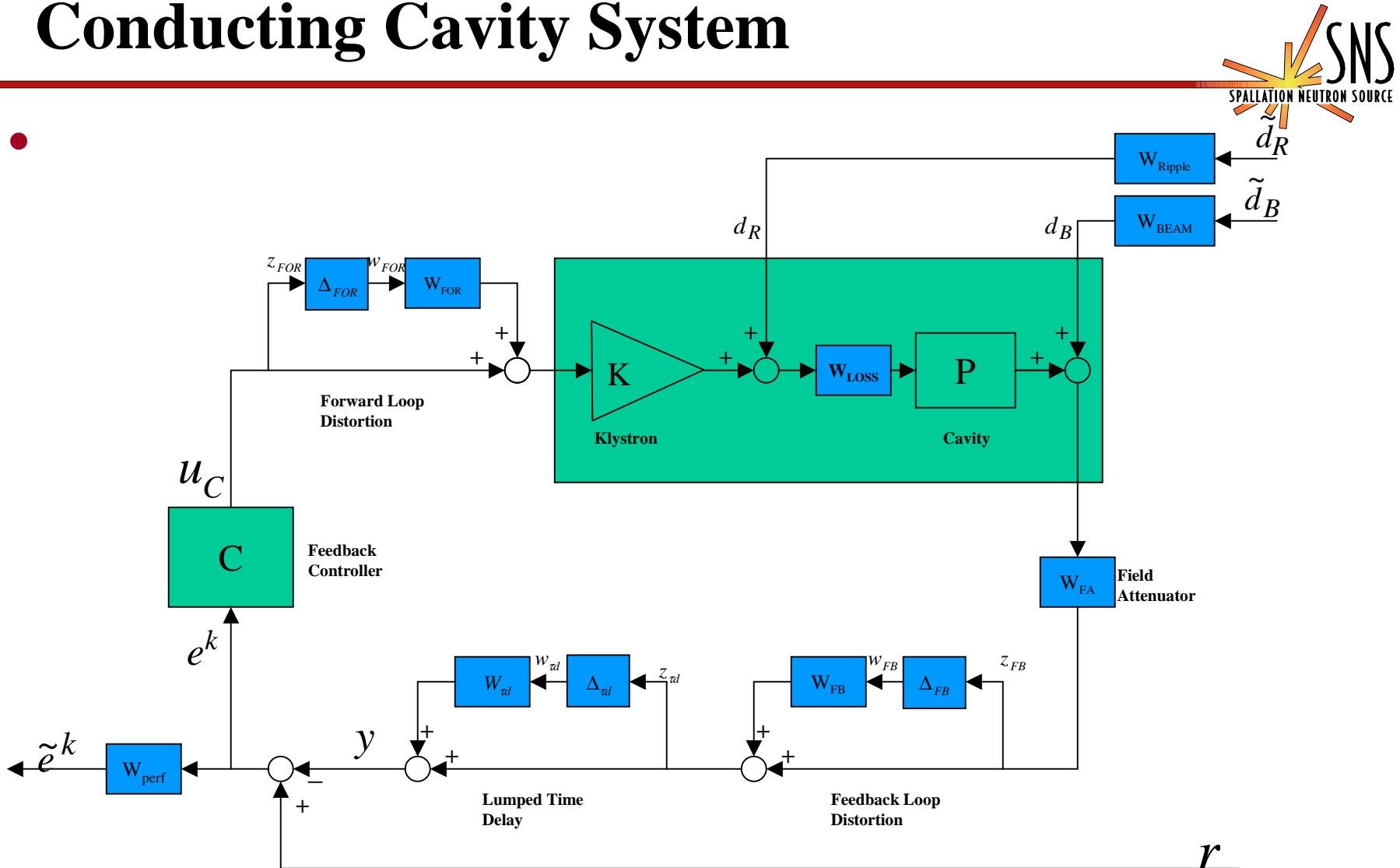
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- Bandwidths
  - Closed Loop System Bandwidth
    - Speed of the Response of the Closed Loop System
    - Determined by the Feedback Controller, Feedforward Controller
    - Disturbance Attenuation Frequency Range
    - Limited By the Loop Time Delays
  - LLRF Control System Bandwidth: Fast hardware,
    - 200 kHz Bandwidth
    - Limitation on FIR Filter Taps because if taps increase, time delay in FIR Filter increases which is against maximizing bandwidth
    - Control System Bandwidth is different from the Closed Loop System Bandwidth

# Uncertainty Model of a Normal Conducting Cavity System

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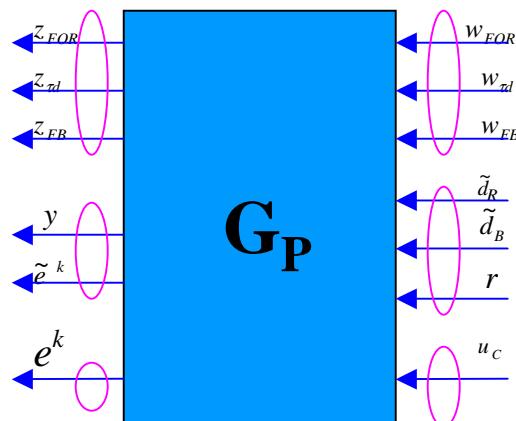
# LFT Representation of the Uncertainty System



- Open Loop System

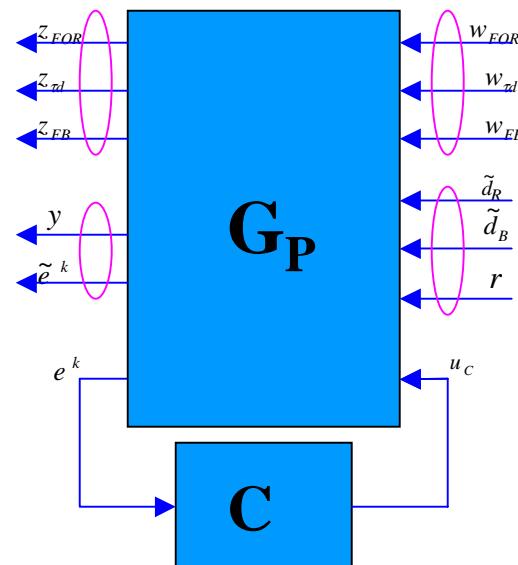
$$\begin{bmatrix} z_{FOR} \\ z_{\pi d} \\ z_{FB} \\ \dots \\ y \\ \tilde{e}^k \\ \dots \\ e^k \end{bmatrix} = G_P \begin{bmatrix} w_{FOR} \\ w_{\pi d} \\ w_{FB} \\ \dots \\ \tilde{d}_R \\ \tilde{d}_B \\ r \\ \dots \\ u_C \end{bmatrix}$$

$$= \begin{bmatrix} G_{11} & : & G_{12} & : & G_{13} \\ \dots & \dots & \dots & \dots & \dots \\ G_{21} & : & G_{22} & : & G_{23} \\ \dots & : & \dots & : & \dots \\ G_{31} & : & G_{32} & : & G_{33} \end{bmatrix} \begin{bmatrix} w_{FOR} \\ w_{\pi d} \\ w_{FB} \\ \dots \\ \tilde{d}_R \\ \tilde{d}_B \\ r \\ \dots \\ u_C \end{bmatrix}$$



- Closed Loop System

$$\begin{bmatrix} z_{FOR} \\ z_{\pi d} \\ z_{FB} \\ \dots \\ y \\ \tilde{e}^k \end{bmatrix} = \begin{bmatrix} G_{CLP11} & : & G_{CLP12} & : & G_{CLP13} \\ \dots & : & \dots & : & \dots \\ G_{CLP21} & : & G_{CLP22} & : & G_{CLP23} \end{bmatrix} \begin{bmatrix} w_{FOR} \\ w_{\pi d} \\ w_{FB} \\ \dots \\ \tilde{d}_R \\ \tilde{d}_B \\ r \end{bmatrix}$$



# Open Loop System Model : Control System with Unity Gain Feedback



- Feedback Loop Distortion
- Time Delay : Feedback Cable+DSP
- Forward Loop Distortion
- FIR Filter

Data Sampling Frequency : 20 MHz

Order : 20

Passband : 1.2 MHz

StopBand : 2.5 MHz

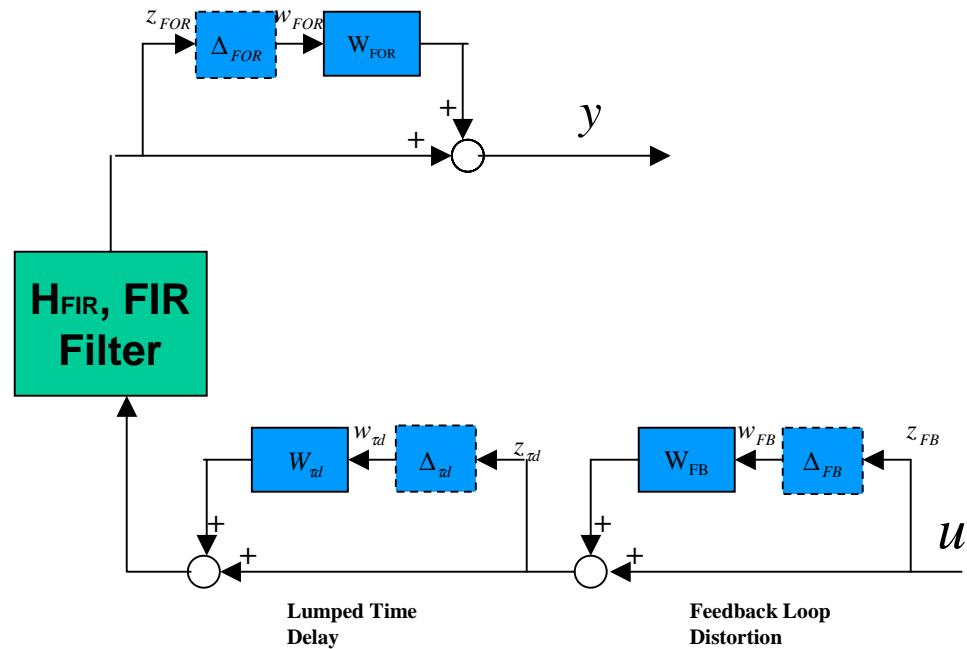
Transient Band : 1.3 MHz

Passband Ripple : 0.5 dB

StopBand Ripple : 37dB

Time Delay : 1.0 usec

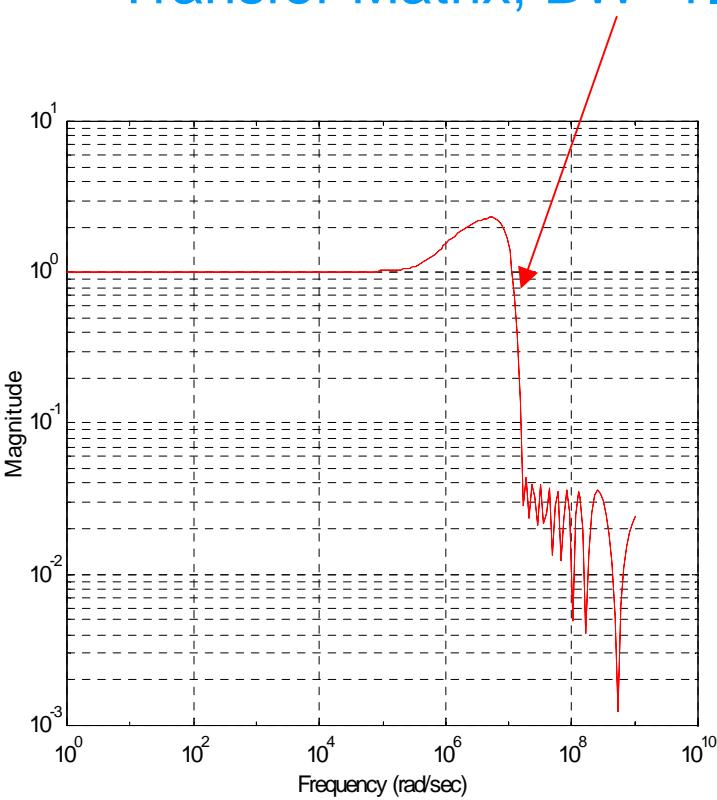
Note that with other parameters fixed, FIR Filter order is inversely proportional to Transient Bandwidth



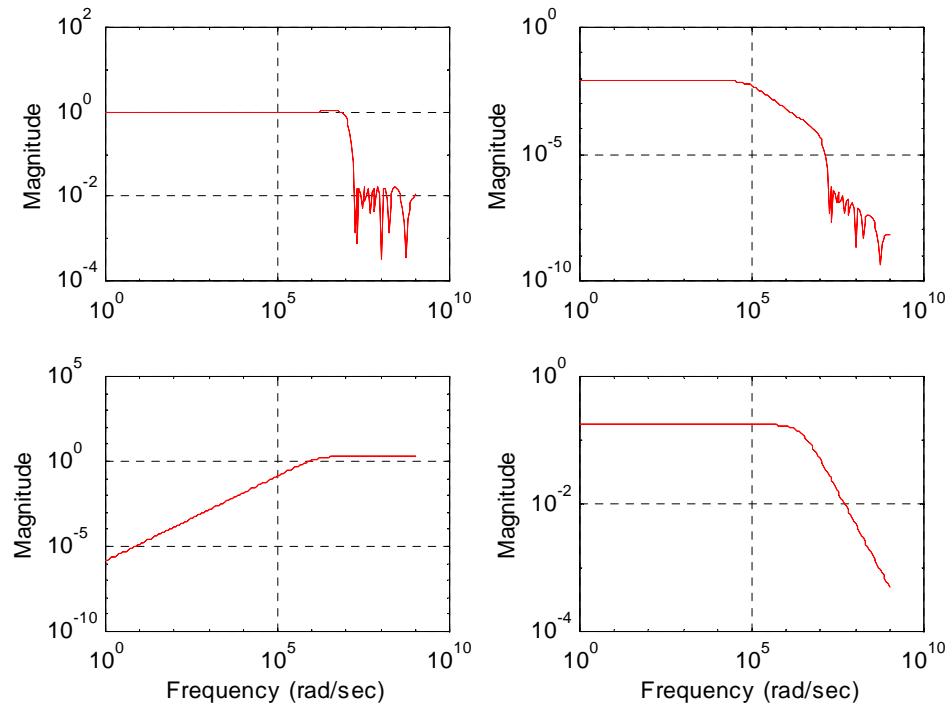
# Frequency Response of Control System with Unity Gain Feedback



- Transfer Matrix, BW=1.596 MHz



Input to Output (Top Left),  
Feedback Loop Distortion to Output (Top Right),  
Time Delay to Output (Bottom Left),  
Forward Loop Distortion to Output (Bottom Right)

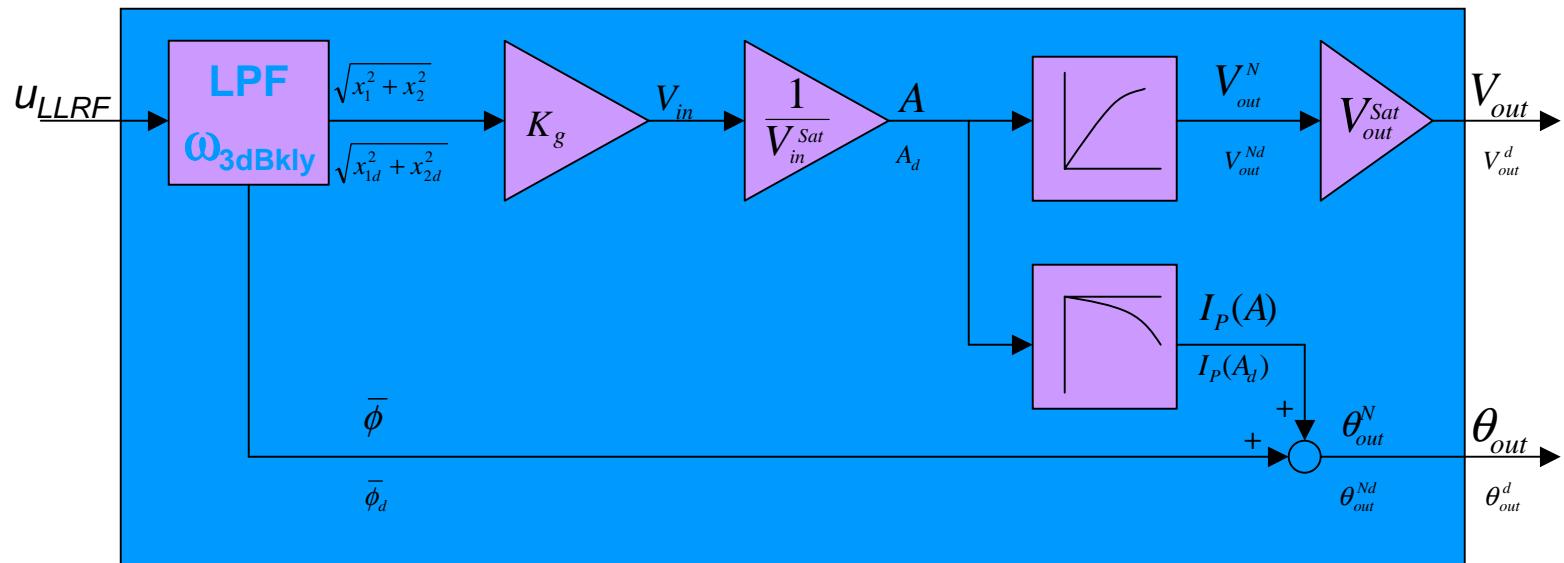


# Open Loop System Model : Klystron

## Block Diagram



- Cascade of linear subsystem and Nonlinear Subsystem
  - Linear Subsystem : Klystron Dynamics,  $\omega_{3dBkly}$
  - Nonlinear Subsystem : Static Saturation Curves

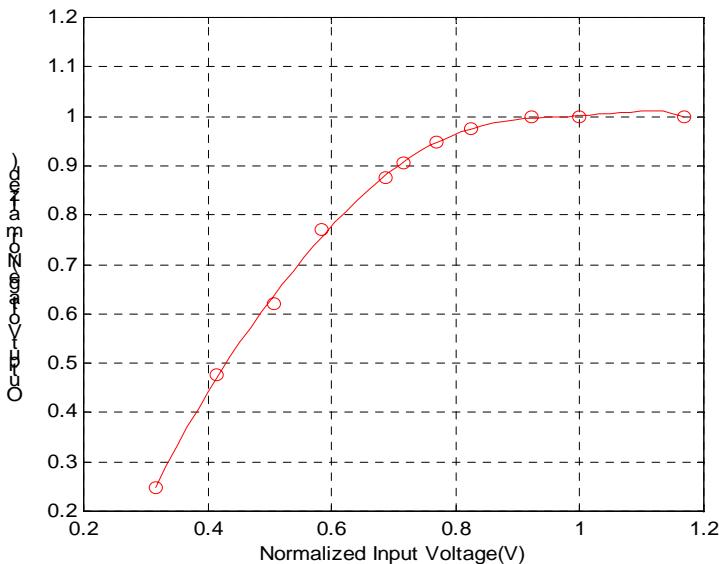


# Klystron Modeling

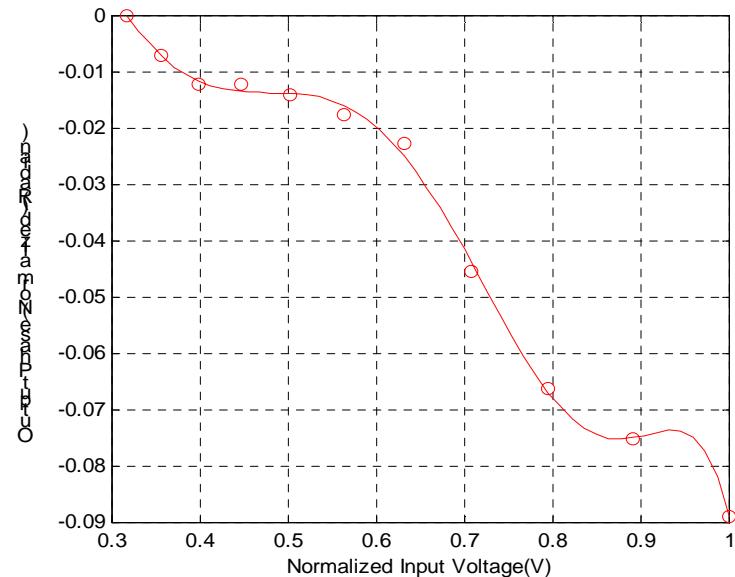
## Nonlinearity



- Amplitude/Phase Saturation Curves



Normalized Amplitude  
Saturation Curve of  
VKP-8290A, 2.5 MW Klystron  
Circle : Measured Data  
Solid Line : Curve Fitting



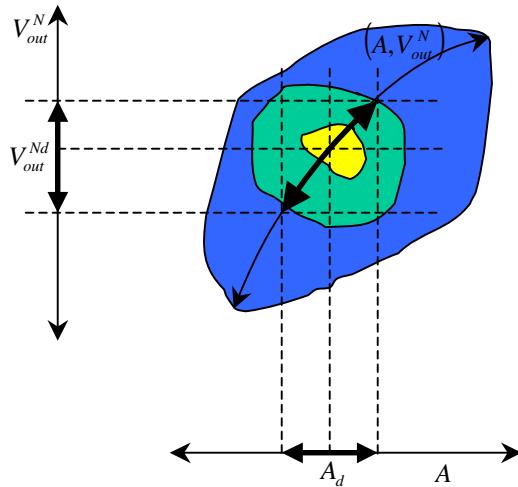
Normalized Phase  
Saturation Curve of  
VKP-8290A, 2.5 MW Klystron  
Circle : Measured Data  
Solid Line : Curve Fitting

# Klystron Modeling

## Linearization



- 1) LPV,      2) Hybrid Model,      3) Lyapunov Linearization



Yellow Region: Lyapunov Linearization  
Green Region: (2.36)-(2.37)  
Blue Region: (2.34)-(2.35)

1)  $\text{[book]} A_k x + B_k u$   
 $y = C_k(A)x$

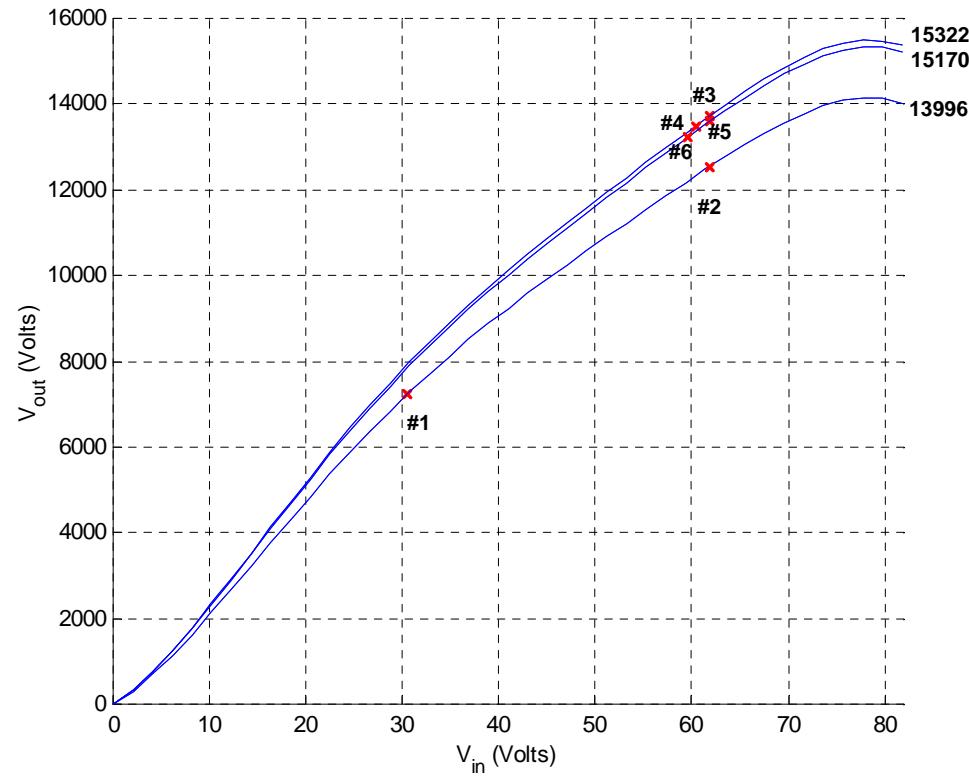
2)  $\text{[book]} A_k x + B_k u$   
 $y = C_k(A_d)x$

3)  $\text{[book]} A_k x_\delta + B_k u_\delta$   
 $y_\delta = C_k(A_d)x_\delta$

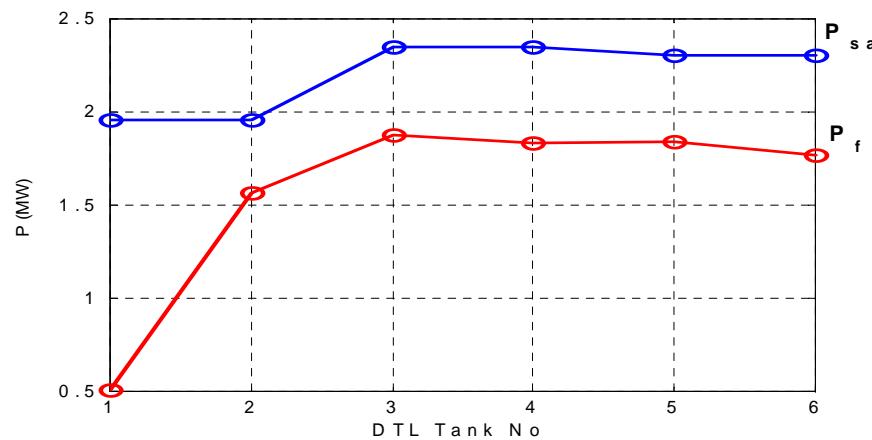
# Control Margin and Saturation Power of Klystrons for 6 DTL Tanks



- Amplitude Saturation Curves and Operating Points

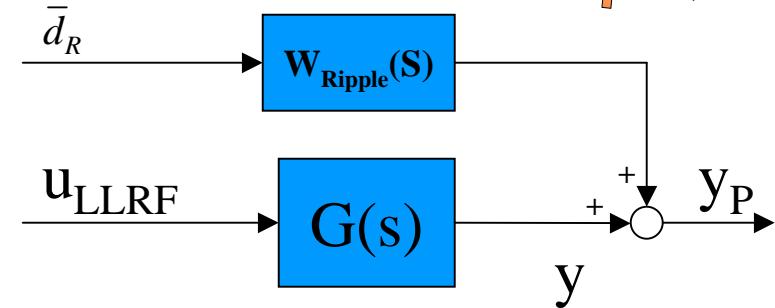
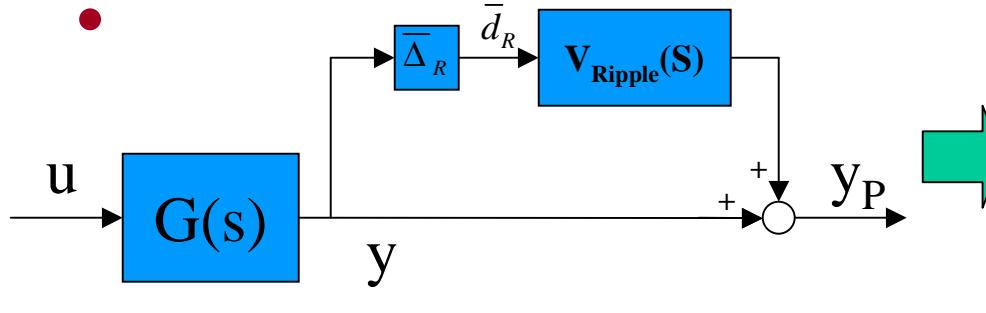


Tank	$P_f$ (MW)	Klystron Operating Point Voltage (kV)	Klystron Saturation Power (MW)	Klystron Saturation Voltage (kV)
1	0.508	7.1274	1.9588	13.9955
2	1.567	12.5180	1.9588	13.9955
3	1.878	13.7040	2.3475	15.3216
4	1.830	13.5277	2.3475	15.3216
5	1.841	13.5683	2.3013	15.1699
6	1.768	13.2966	2.3013	15.1699



# Open Loop System Model : HVPS Ripple in Klystron

(1.2 % Amplitude Ripple, 11.5 Degree Phase Ripple)

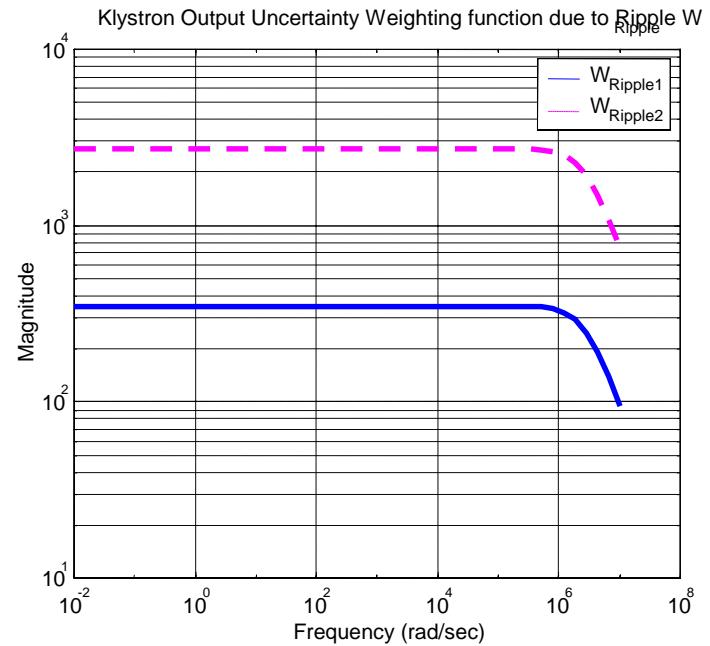


$$Y_P(S) = G(s)U_{LLRF}(s) + W_{Ripple}(s)\bar{d}_R(s)$$

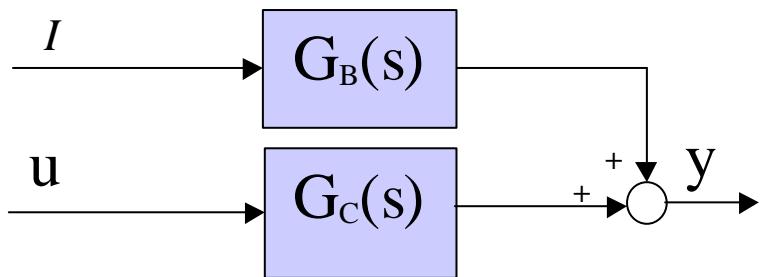
$W_{Ripple}(s)$  : Transfer Function from Ripple to Klystron Output

$$W_{Ripple}(s) = \begin{bmatrix} w_{Ripple1}(s) & 0 \\ 0 & w_{Ripple2}(s) \end{bmatrix}$$

$$\|\bar{\Delta}_R(\omega)\|_\infty \leq 1, \quad \forall \omega$$



# Open Loop System Model : NC Cavity with BEAM Dynamics



$$\begin{aligned} & A_c z + B_z u + B_{zI} I \\ y = Cz \end{aligned}$$

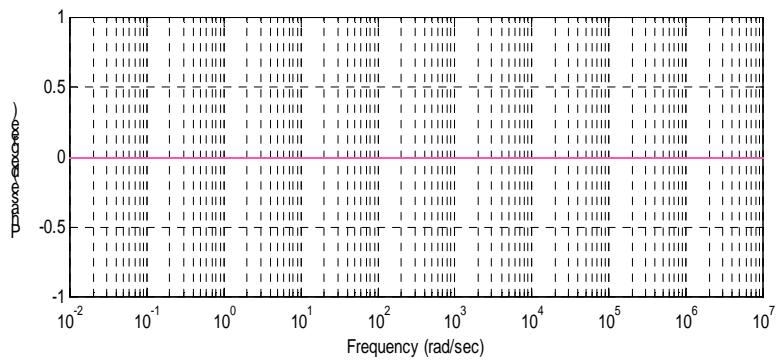
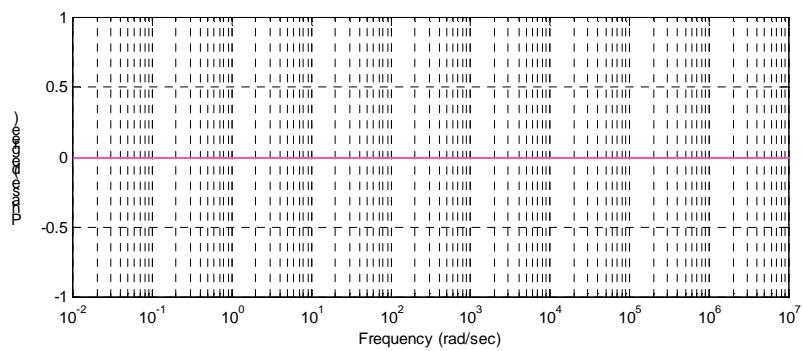
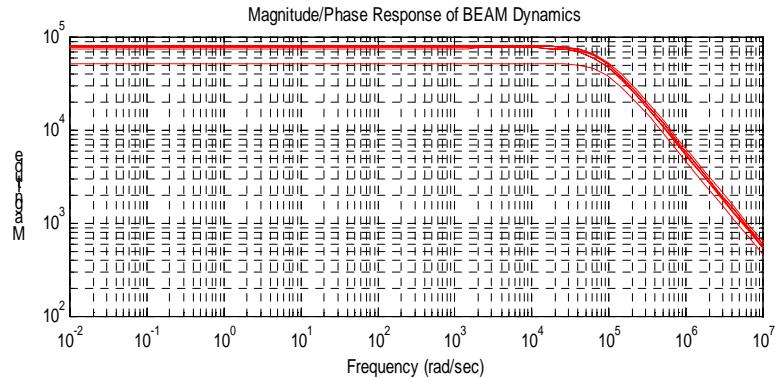
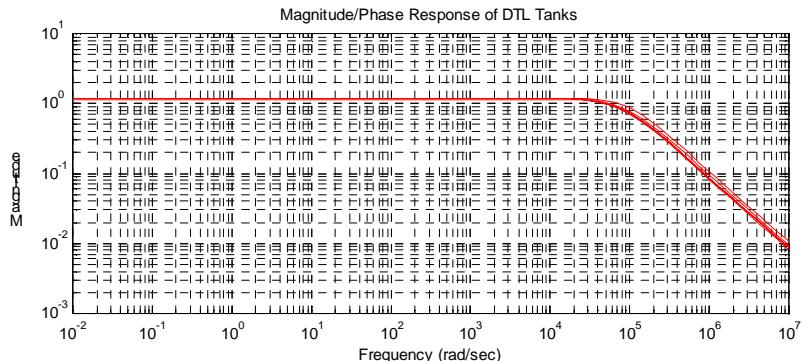
$$\forall M, \quad B_{zI} = M B_z$$

$$Y(s) = G_c(s)U(s) + G_B(s)I(s)$$

$$G_c(s) = C_z (sI - A_z)^{-1} B_z$$

$$G_B(s) = C_z (sI - A_z)^{-1} B_{zI}$$

# Frequency Response of NC Cavity with BEAM Dynamics



$$G_c(s) = C_z (sI - A_z)^{-1} B_z$$

**Bandwidth=[11.3kHz 14.1 kHz]**

$$G_B(s) = C_z (sI - A_z)^{-1} B_{zI}$$

# Closed Loop System



- Open Loop System

$$G_o = e^{-s\tau d} H_{FIR} W_{FA} G_C G_K$$

- Lumped Loop Delay :  $\tau_d = 1.392 \mu \text{ sec}$
- Feedback Controller : PI Controller   
**K<sub>p</sub>=5 I**  
**K<sub>i</sub>=1,000,000 I**

- The Large PI gains yield the Peaking in Frequency Responses around 80 kHz, which can be avoided by reducing gains with the sacrifice of the closed loop system bandwidth
- Remark: When K<sub>p</sub>=2.5 I, K<sub>i</sub>=100,000 I, then the peaking is reduced less than 1.2 but the closed loop system bandwidth is 19.9 kHz, which increases the necessity of feedforward Control to improve the transient behaviors for RF filling and beam loading

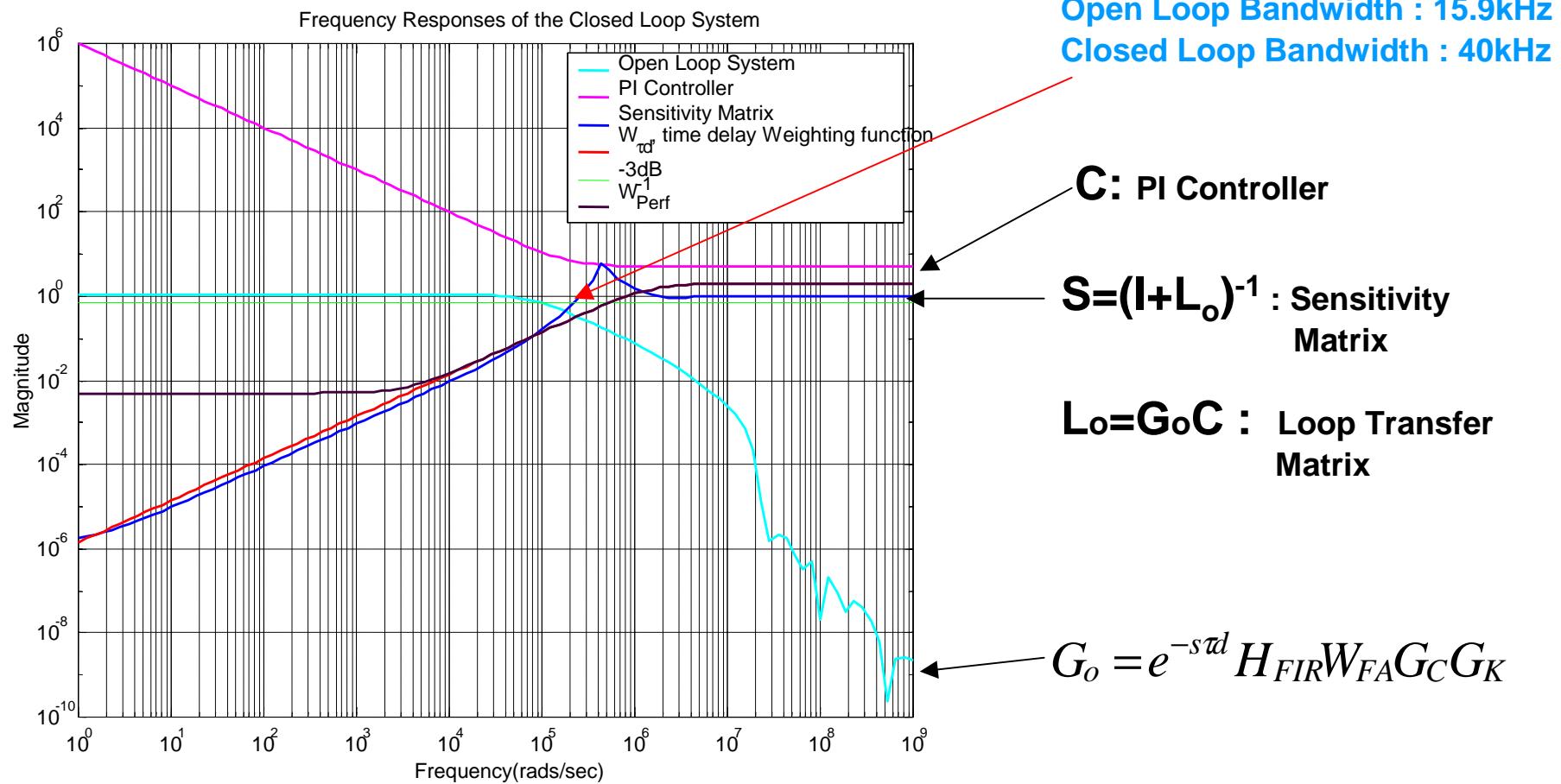
- Bandwidths

- DTL : 11.7 kHz (Q<sub>L</sub>:17247 (DTL Tank 3))
- Control System Bandwidth : 1.56 MHz
- Klystron Bandwidth : 600 kHz (assumed)
- [Open Loop System Bandwidth : 15.9 kHz](#)
- [Closed Loop System Bandwidth : 40.0 kHz](#)

# Closed Loop System with PI Controller

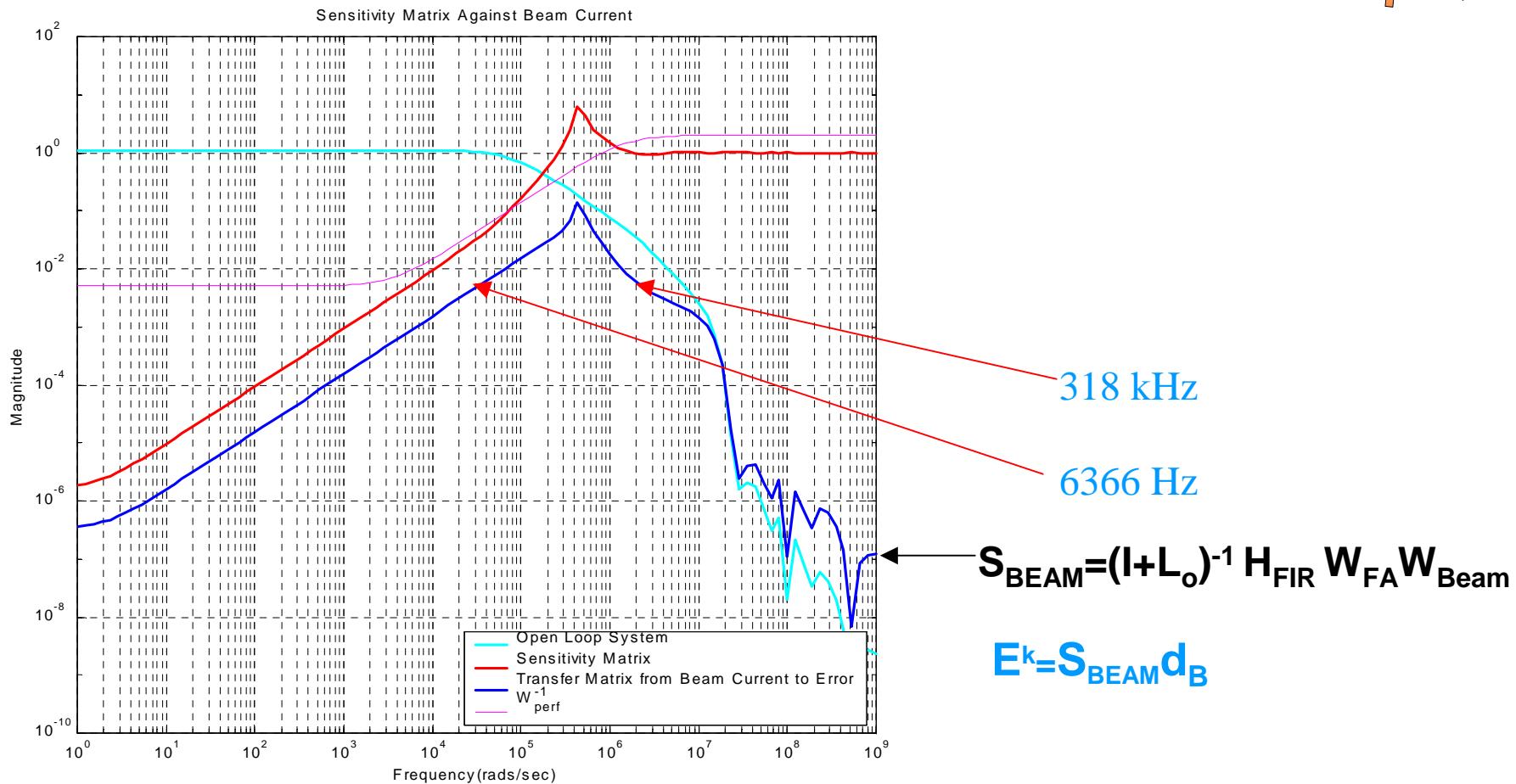
Sensitivity Matrix,  $S : E^k = S_r$ ,

Complementary Sensitivity Matrix,  $T : y = T_r$



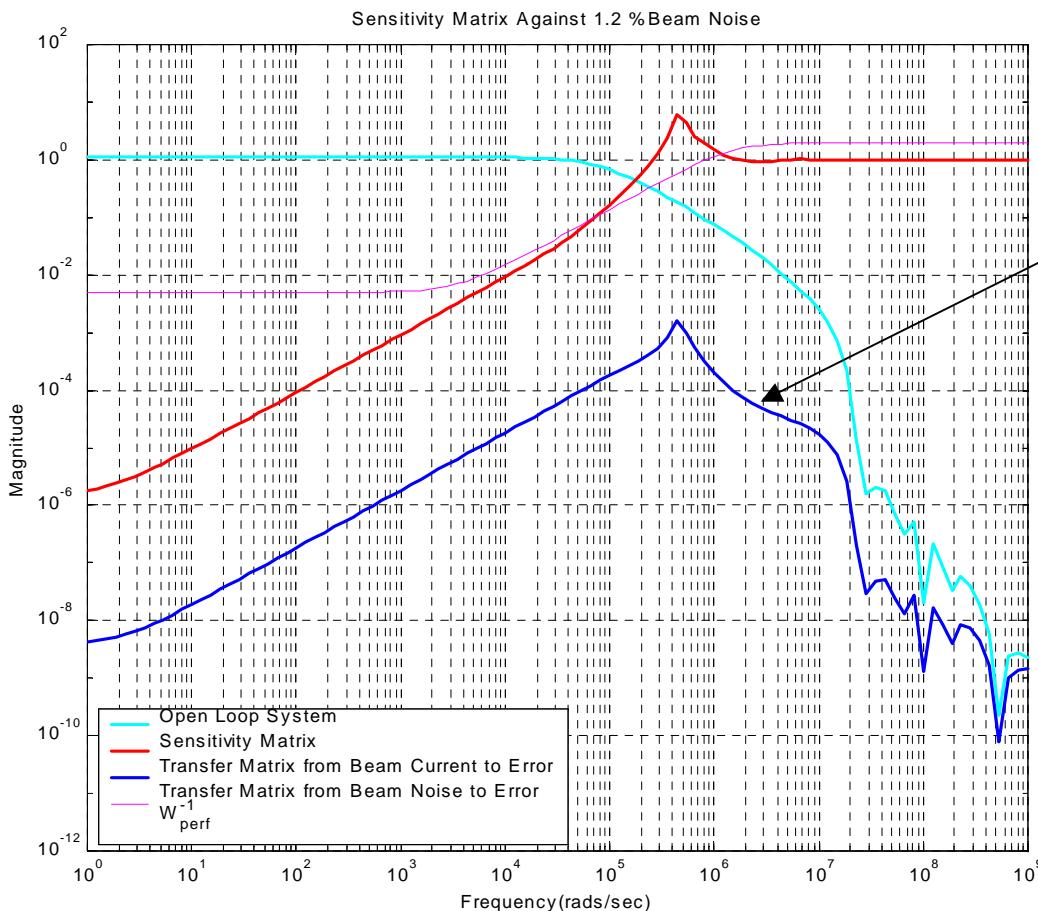
# Closed Loop System

## Sensitivity Matrix to BEAM CURRENT, $S_{\text{BEAM}}$



# Closed Loop System

Sensitivity Matrix to 1.2 % Beam Noise,  $S_{BN}$

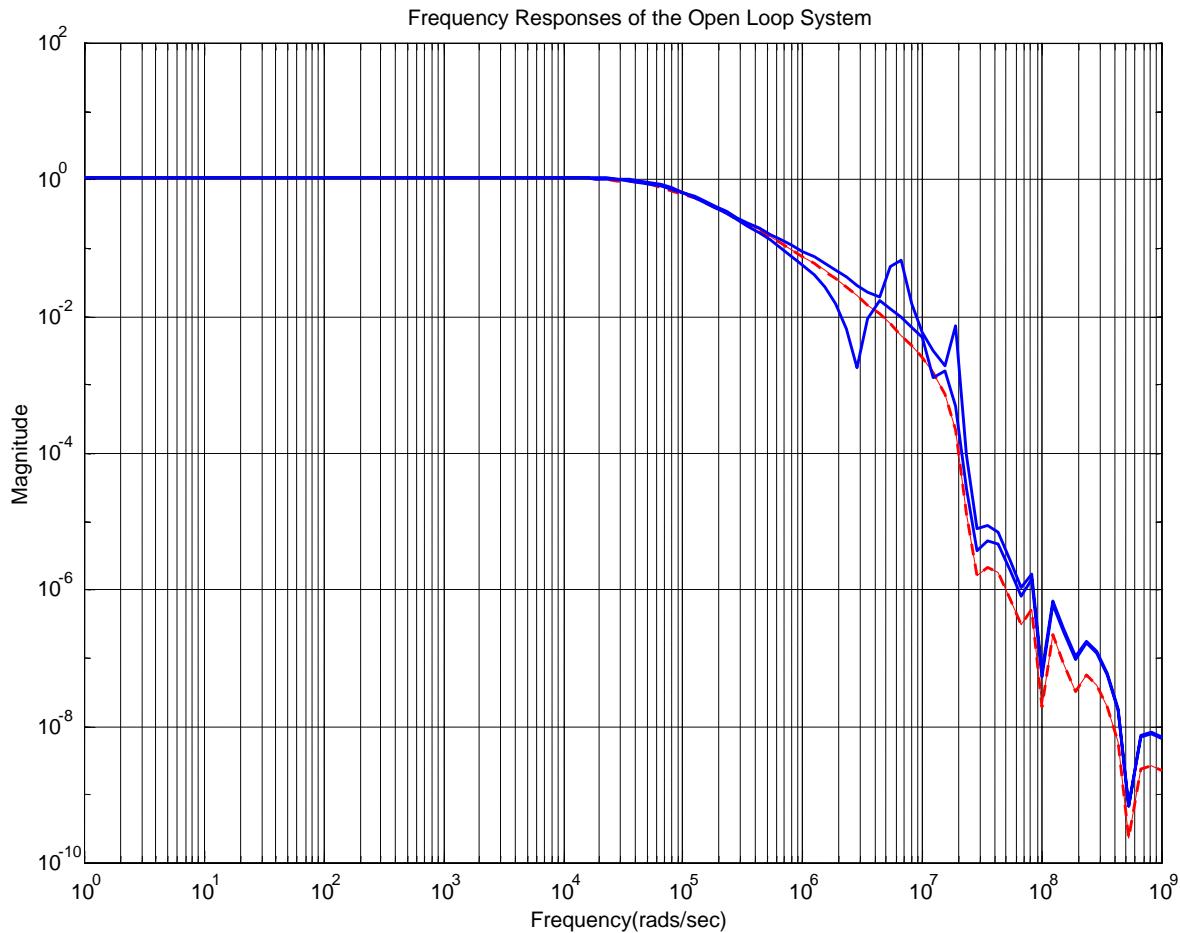


$$S_{BN} = (I + L_o)^{-1} H_{FIR} W_{FA} W_{Beam} I_{0.012}$$

$$I_{0.012} = 0.012 I$$

$$E^k = S_{BN} B_{NS}$$

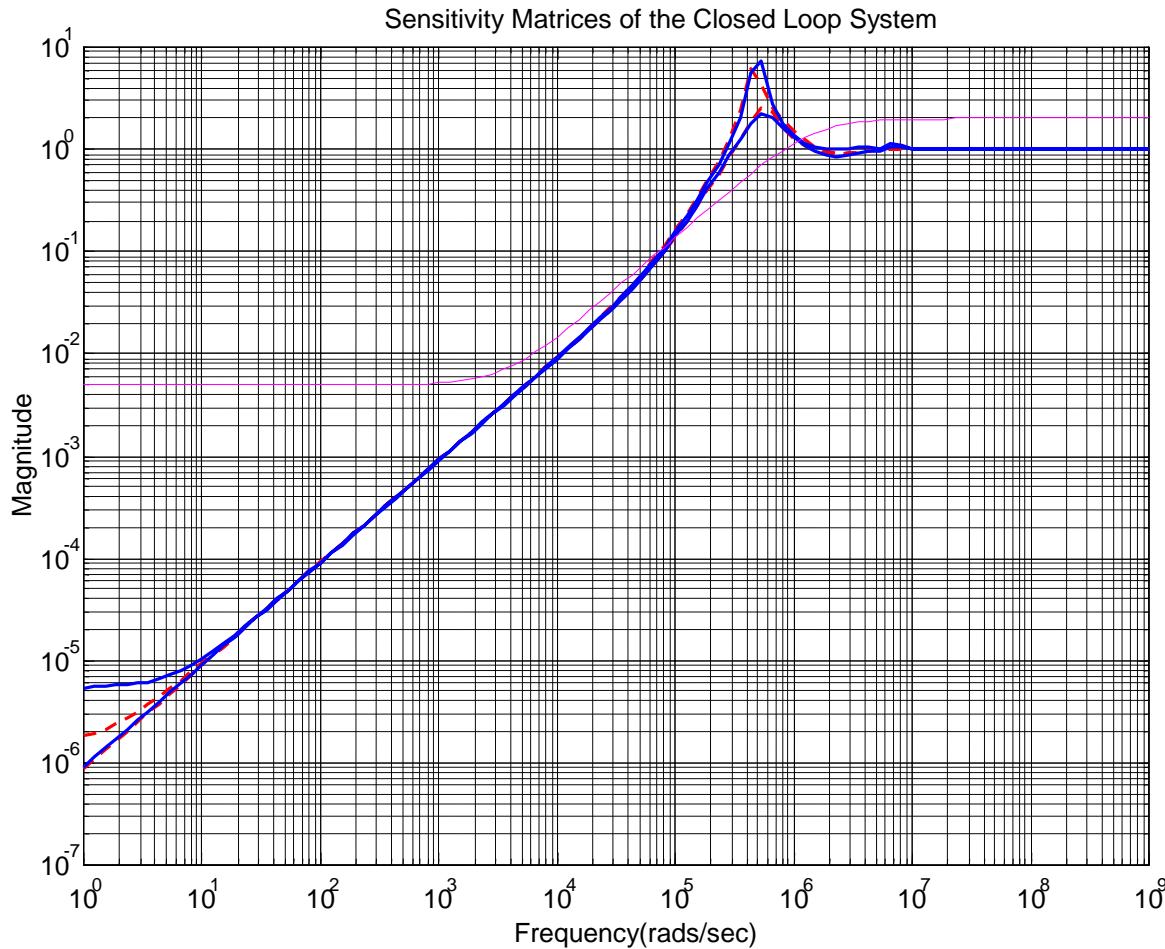
# Open Loop System With Other Modes



DTL TANK 3  
33 Drift Tubes  
Near Modes :  
0.99 MHz  
2.89 MHz

# Closed Loop System

## Sensitivity Matrix With Other Modes



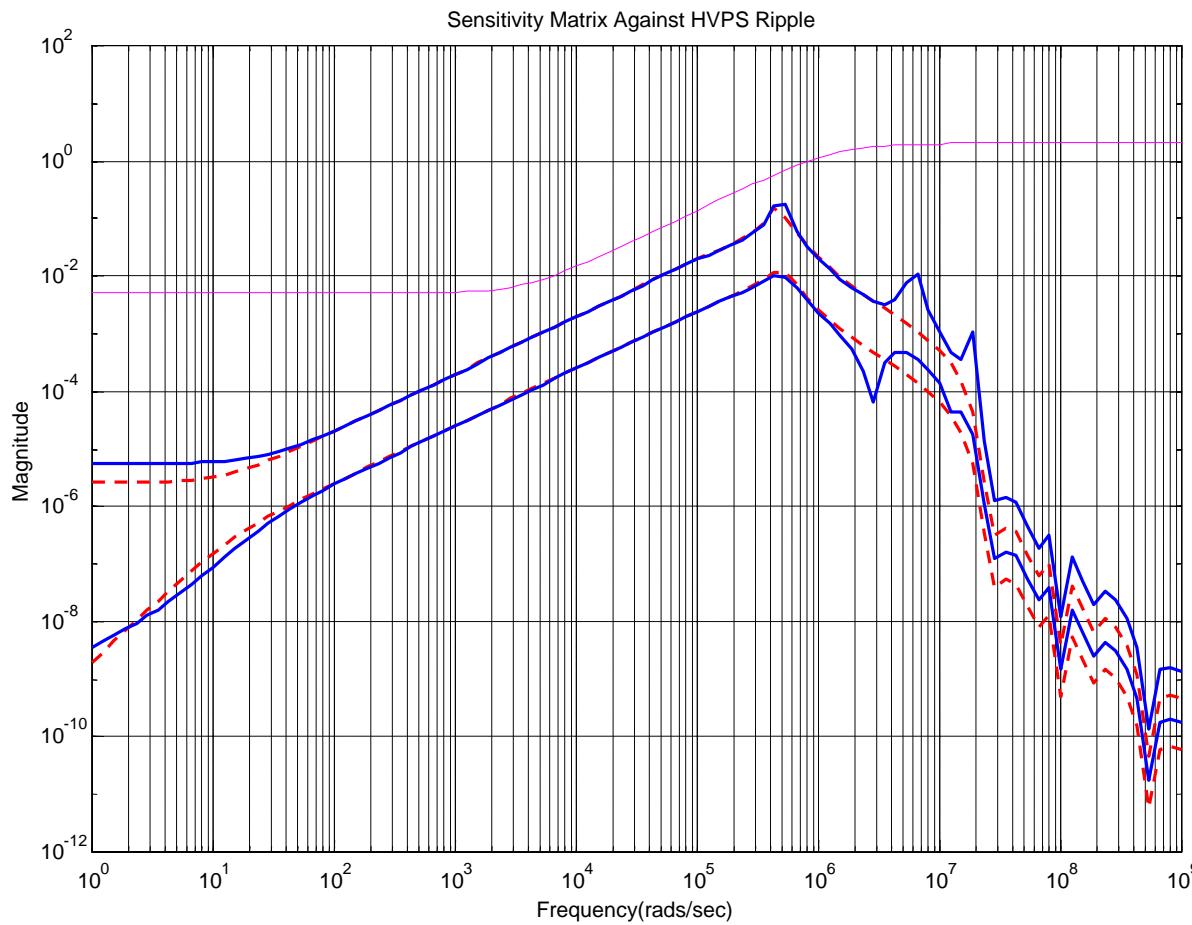
Dashed Line : Single Mode

Solid Line : 3 Modes

# Closed Loop System

Sensitivity Matrix With Other Modes to

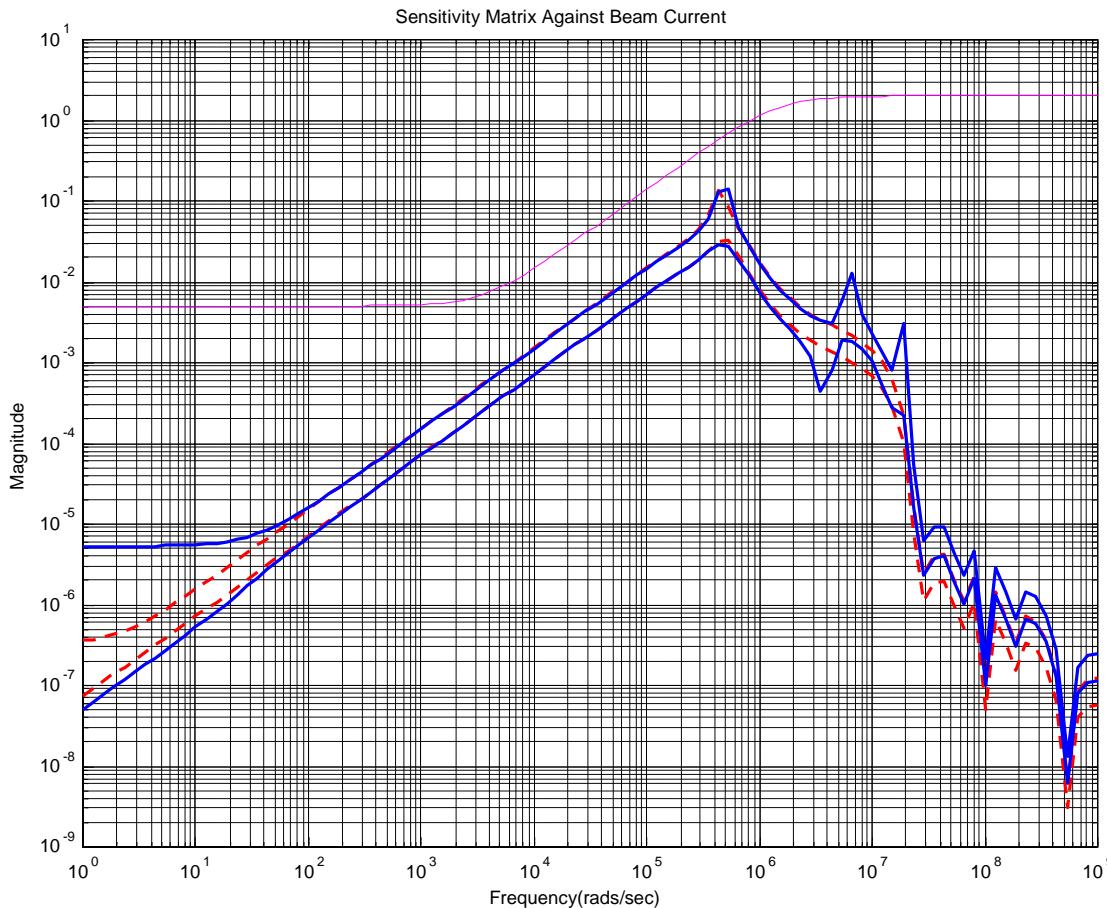
HVPS Ripple (1.2 % Amplitude Ripple, 11.5 Degree Phase Ripple)



DTL TANK 3  
33 Drift Tubes  
Near Modes :  
0.99 MHz  
2.89 MHz

# Closed Loop System

## Sensitivity Matrix With Other Modes to Beam Current

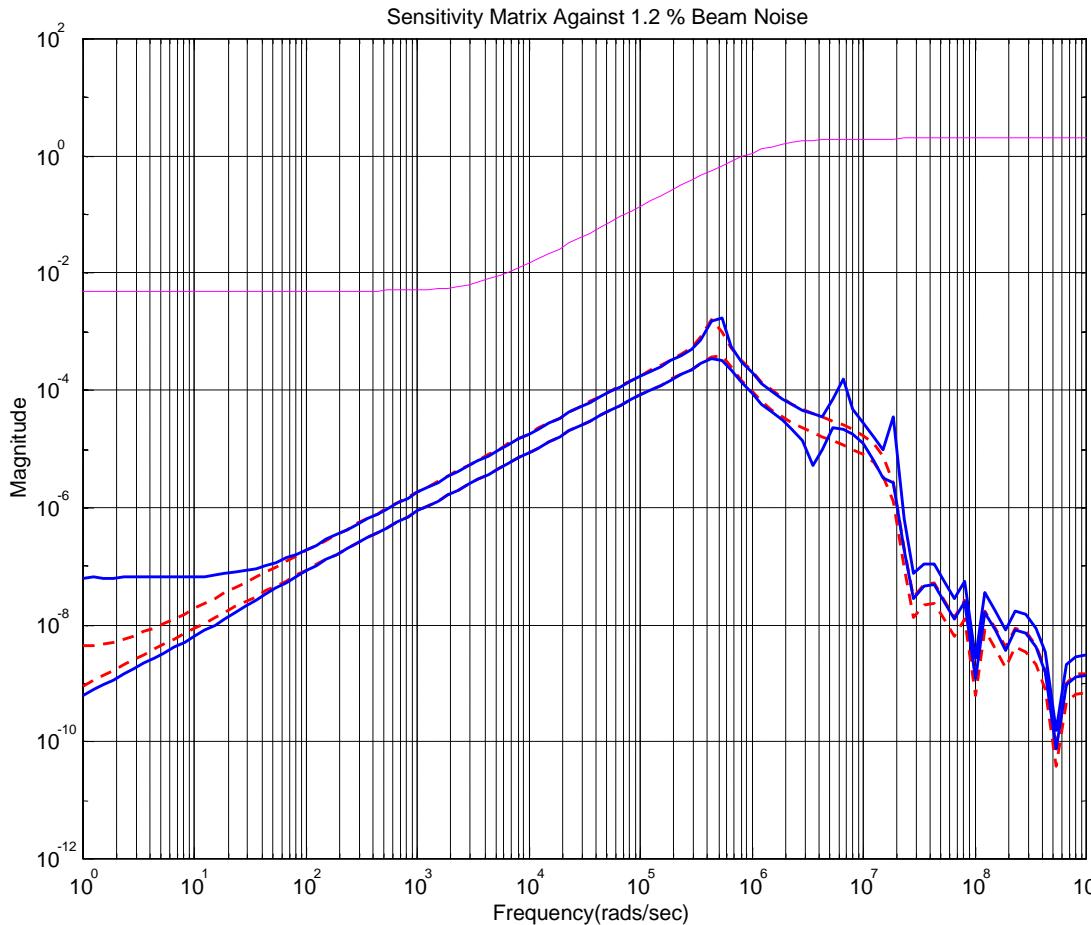


DTL TANK 3  
33 Drift Tubes  
Near Modes :  
0.99 MHz  
2.89 MHz

Dashed Line : Single Mode  
Solid Line : 3 Modes

# Closed Loop System

Sensitivity Matrix With Other Modes to  
1.2 % Beam Noise



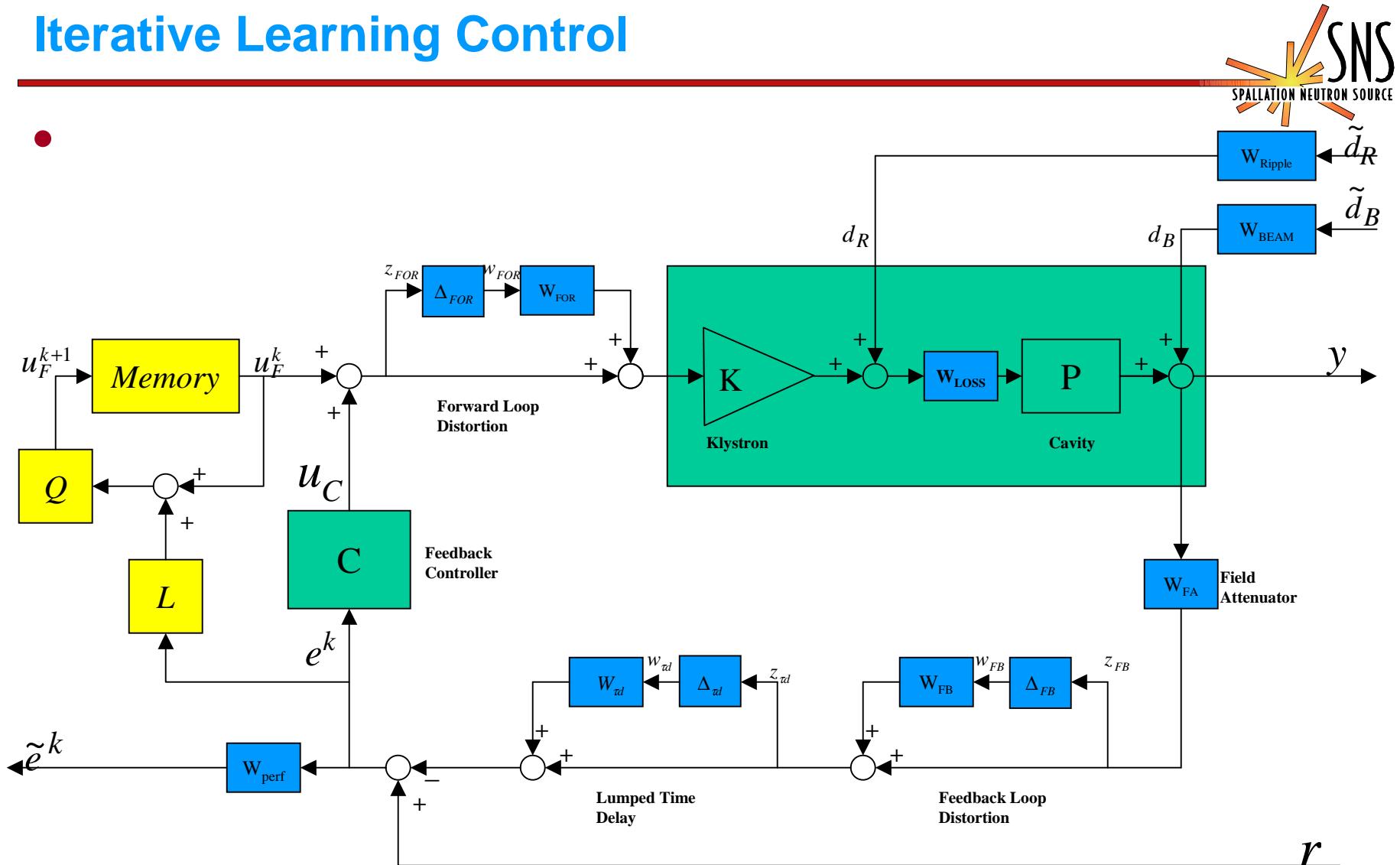
DTL TANK 3  
33 Drift Tubes  
Near Modes :  
0.99 MHz  
2.89 MHz

Dashed Line : Single Mode  
Solid Line : 3 Modes

# Feedforward Control

## Iterative Learning Control

- 



# Feedforward Controller

## Iterative Learning Controller



- $U_F^{k+1} = Q \left( f \cdot U_F^k + \alpha \cdot LE^k \right)$

$$\|Q(s)(f \cdot I - \alpha \cdot L(s)G_L(s, \Delta\omega_L, A_d))\|_{\infty} < 1$$

$$G_L(s, \Delta\omega_L, A_d) = T(s, \Delta\omega_L, A_d)C^{-1}(s)$$

$$\lim_{k \rightarrow \infty} E^k = (I + CP)^{-1} R$$

Filter  $L(s)$  : Solution of Chebycheff Approximation

$$\min \max_{i=0, \dots, N} \bar{\sigma}(G_L(\omega_i, \Delta\omega_L, A_d) - \hat{G}_L(\omega_i))$$

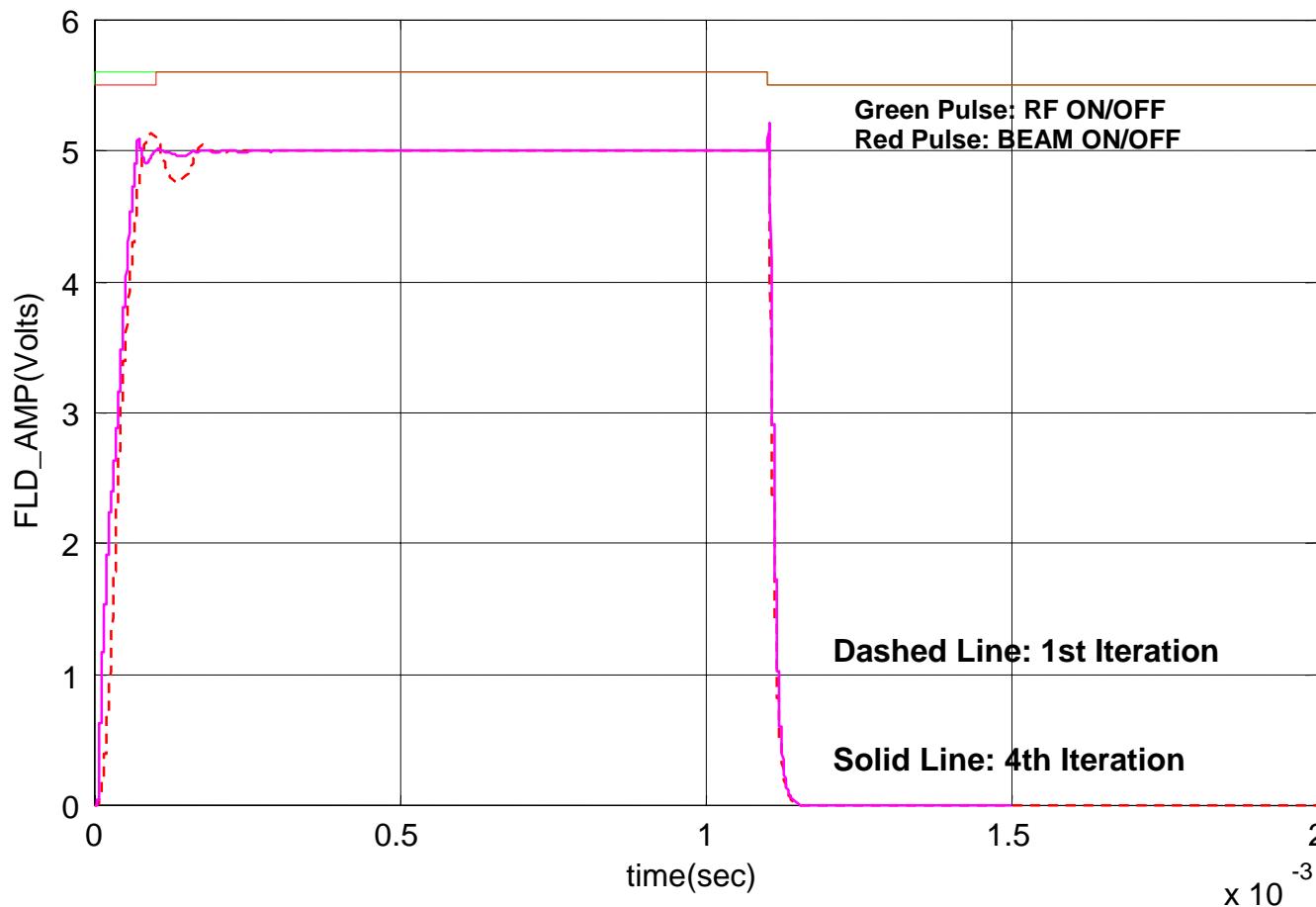
$$\hat{G}_L(s) = \begin{bmatrix} \hat{G}_{LI}(s) & 0 \\ 0 & \hat{G}_{LQ}(s) \end{bmatrix}$$

$$\hat{G}_{LI}(s) = \frac{s}{a_{I2}s^2 + a_{I1}s + a_{I0}}$$

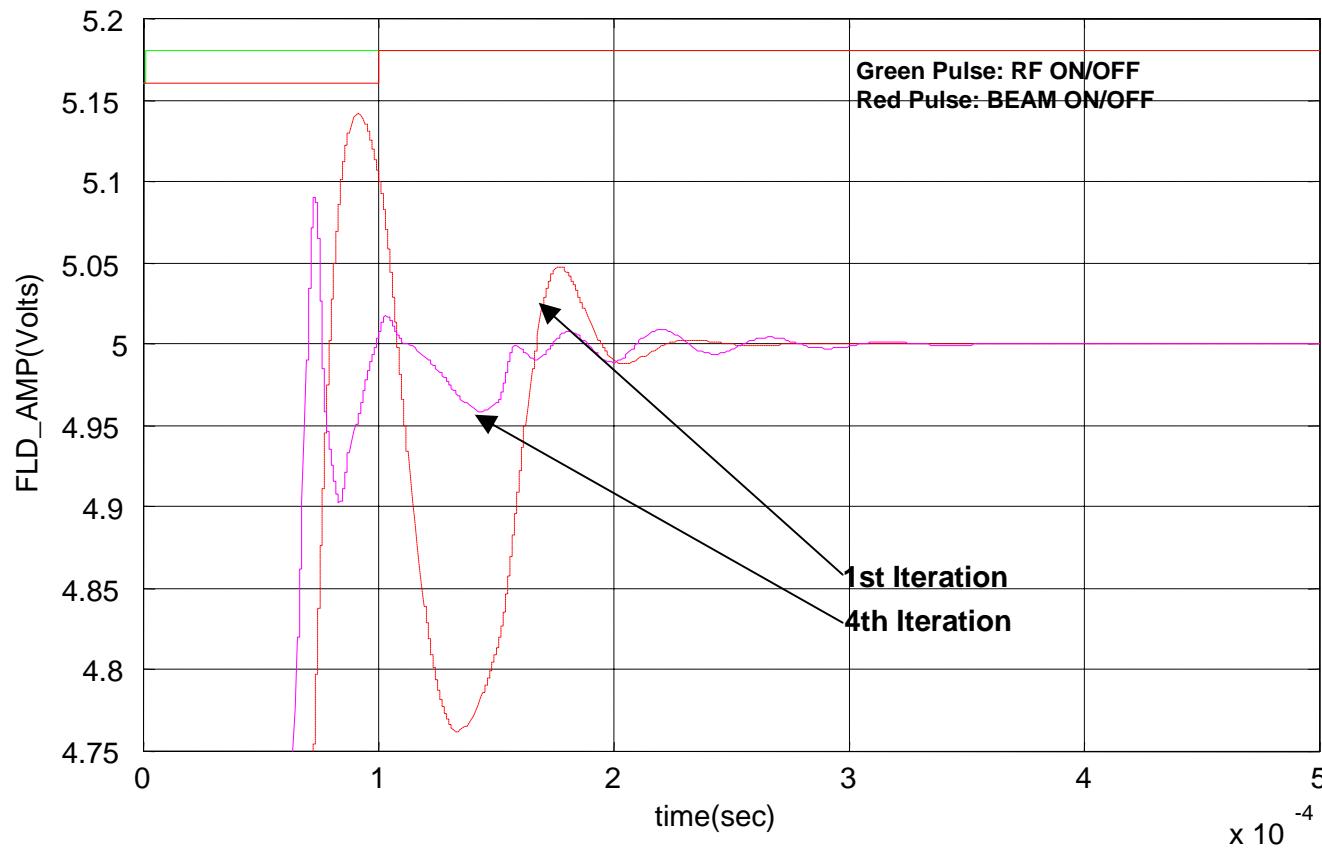
$$\hat{G}_{LQ}(s) = \frac{s}{a_{Q2}s^2 + a_{Q1}s + a_{Q0}}$$

# Feedback+Feedforward Controller

## Field Amplitude

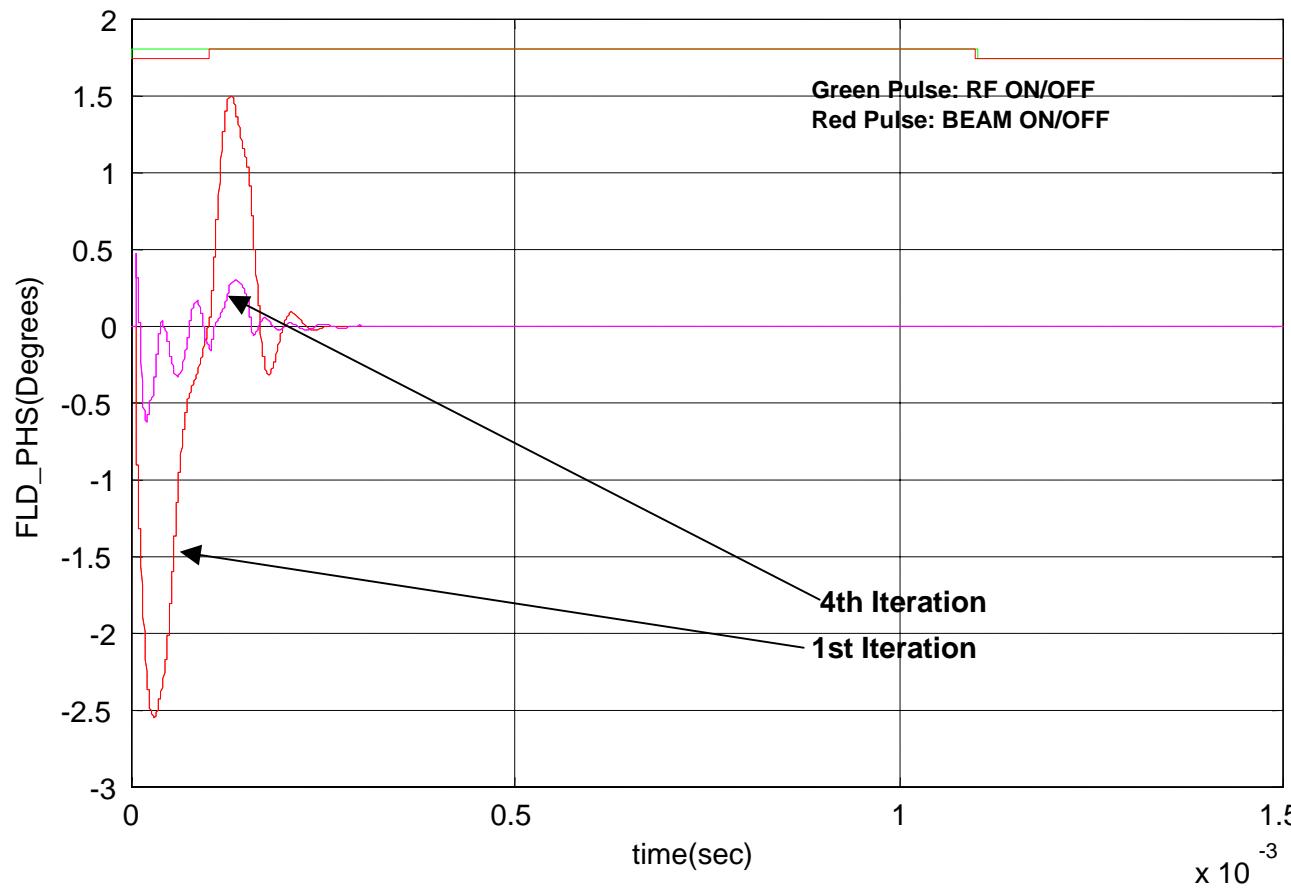


# Zoom of Field Amplitude

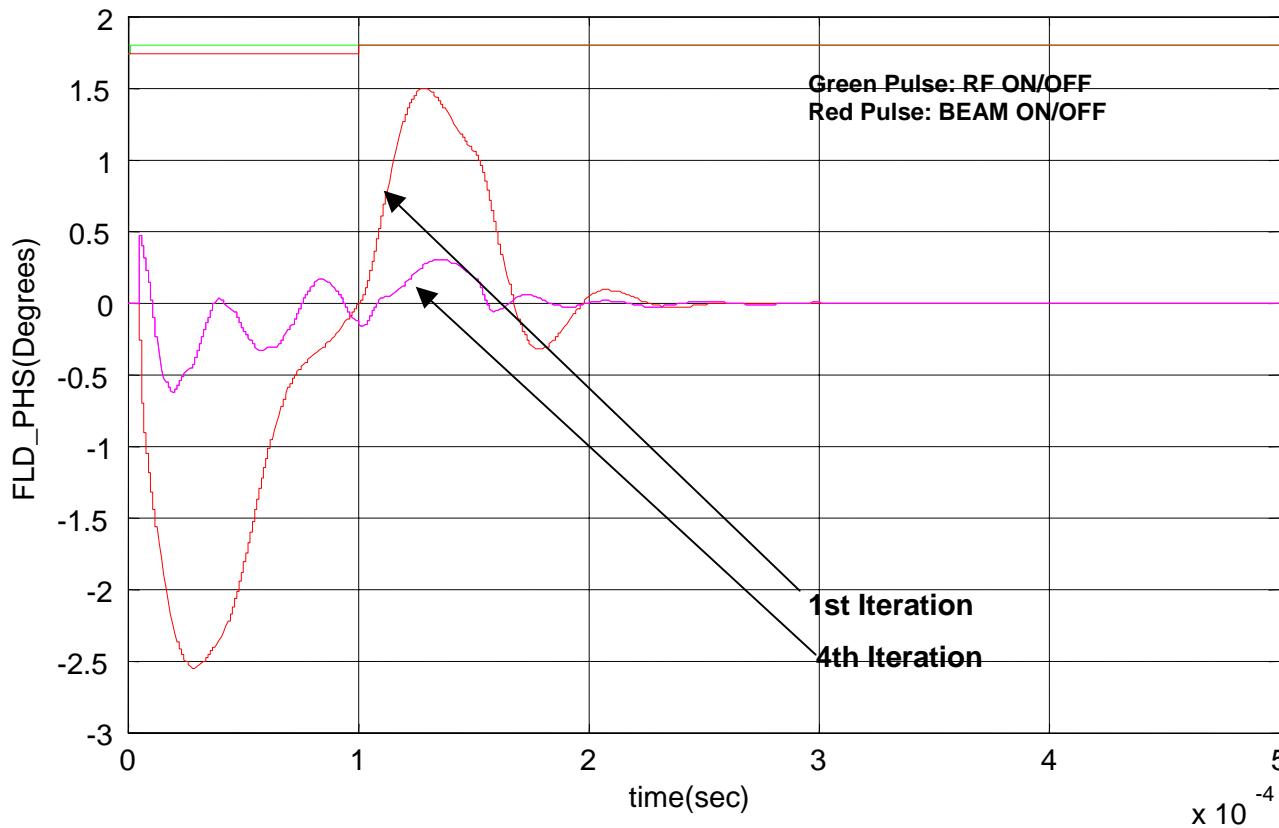


# Feedback+Feedforward Controller

## Field Phase



# Zoom of Field Amplitude



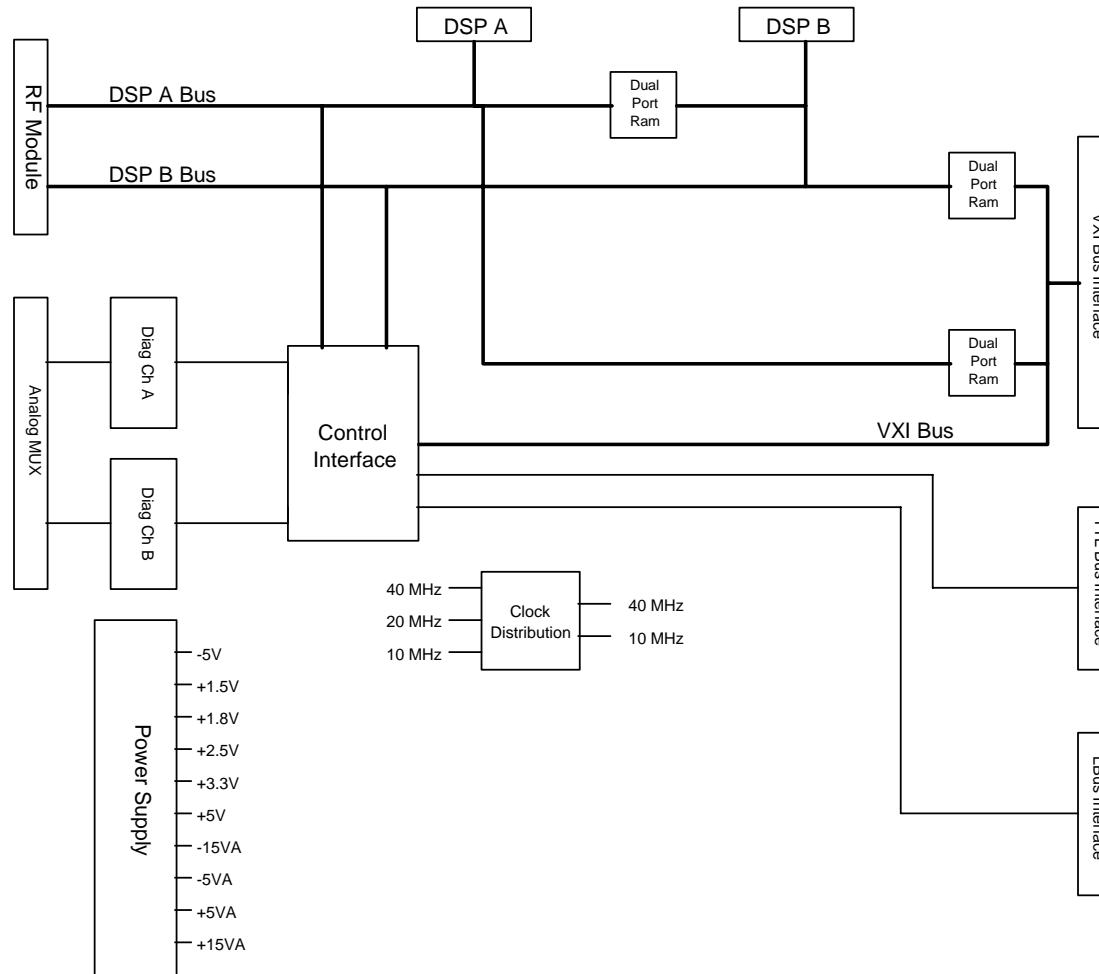
# Motherboard Requirements

---

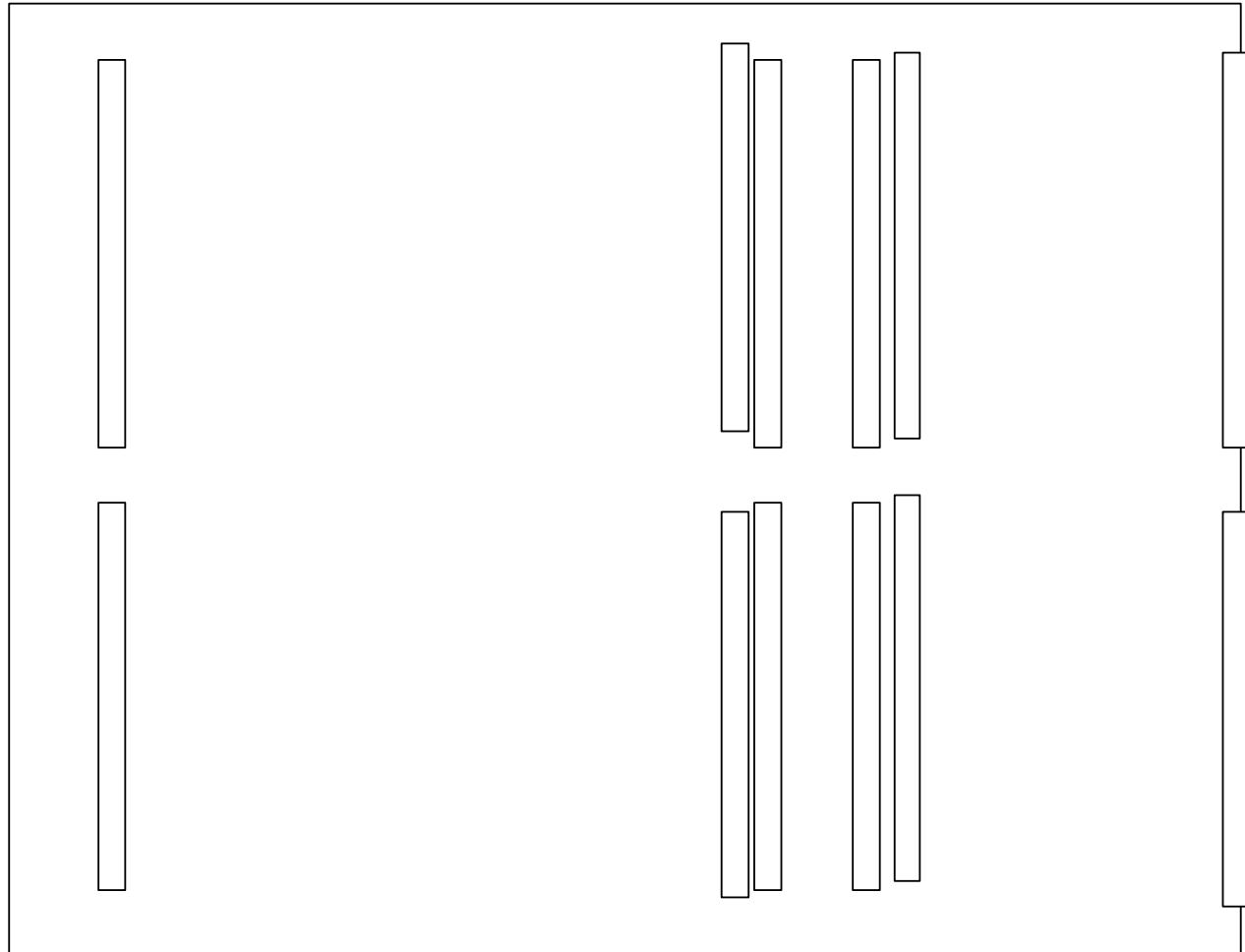


- VXIbus Interface
- P2 Bus Interface
- Module Interface and Communications
- On-board Clock Distribution
- Power Generation and Distribution
- Diagnostic Circuitry

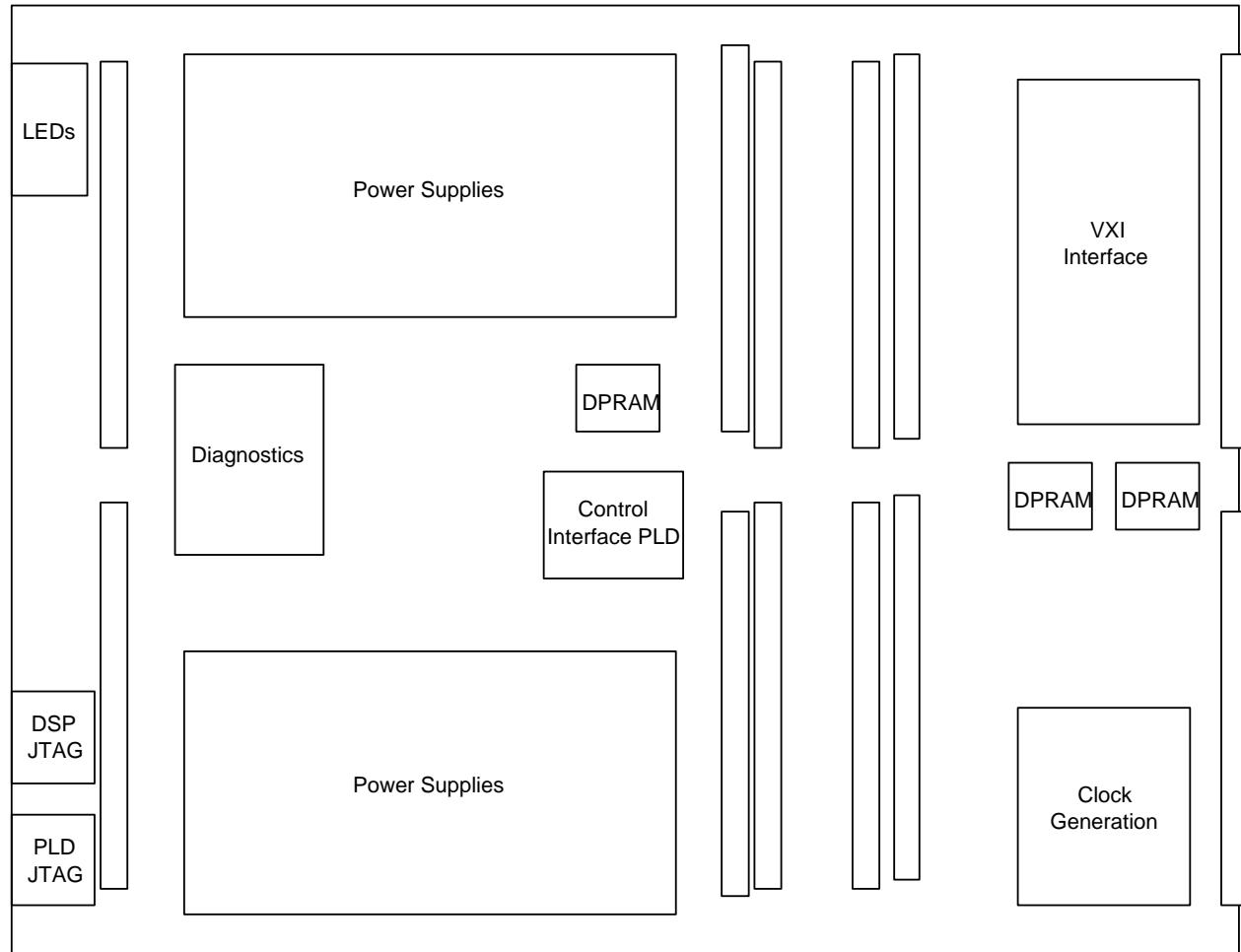
# Motherboard Functional Diagram



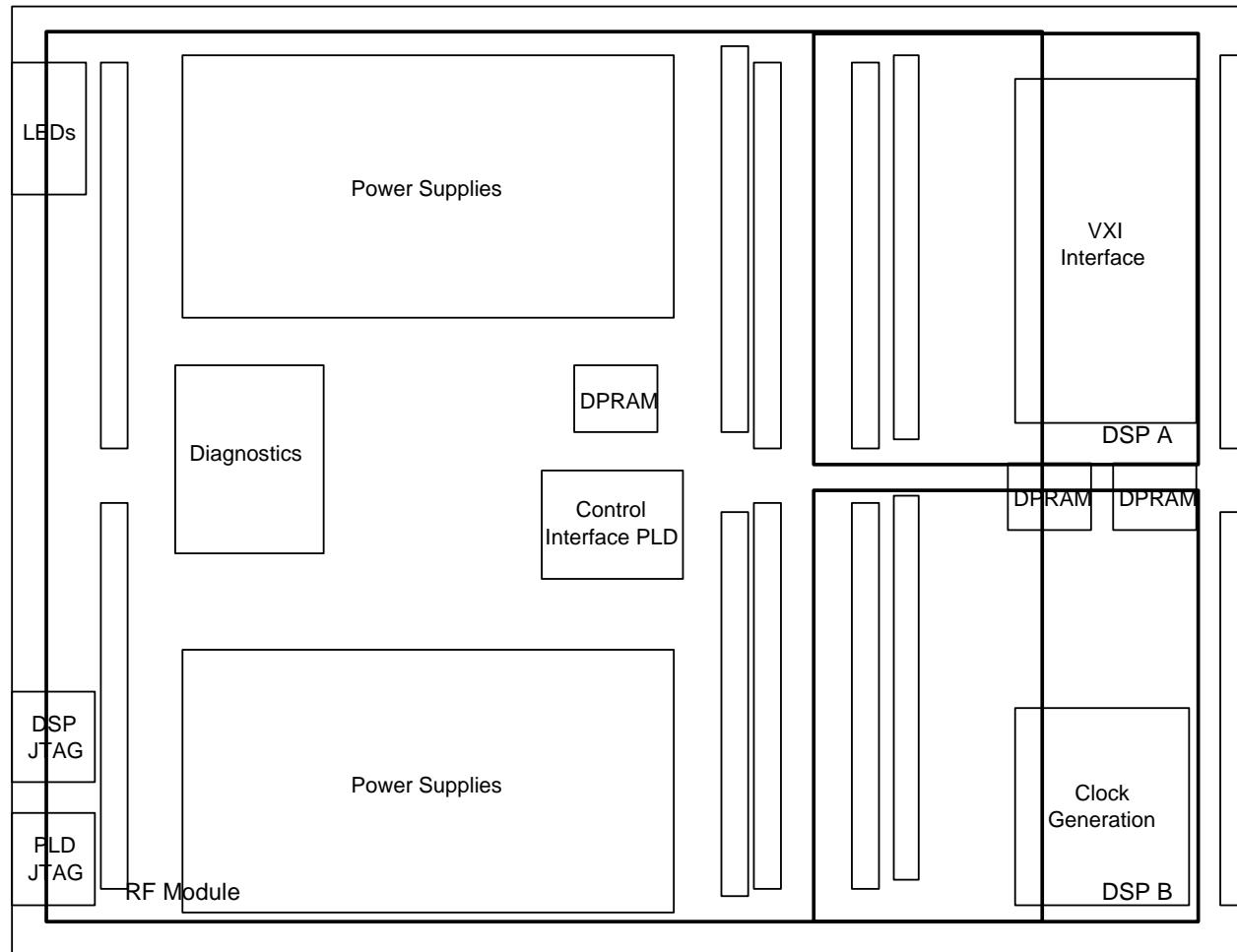
# Motherboard Physical I



# Motherboard Physical II



# Motherboard Physical III



# Motherboard Design Status



- Schematics in check phase
- Completing PLD design for pinout
  - 25% Complete
  - Preparing simulations
- Parts list complete

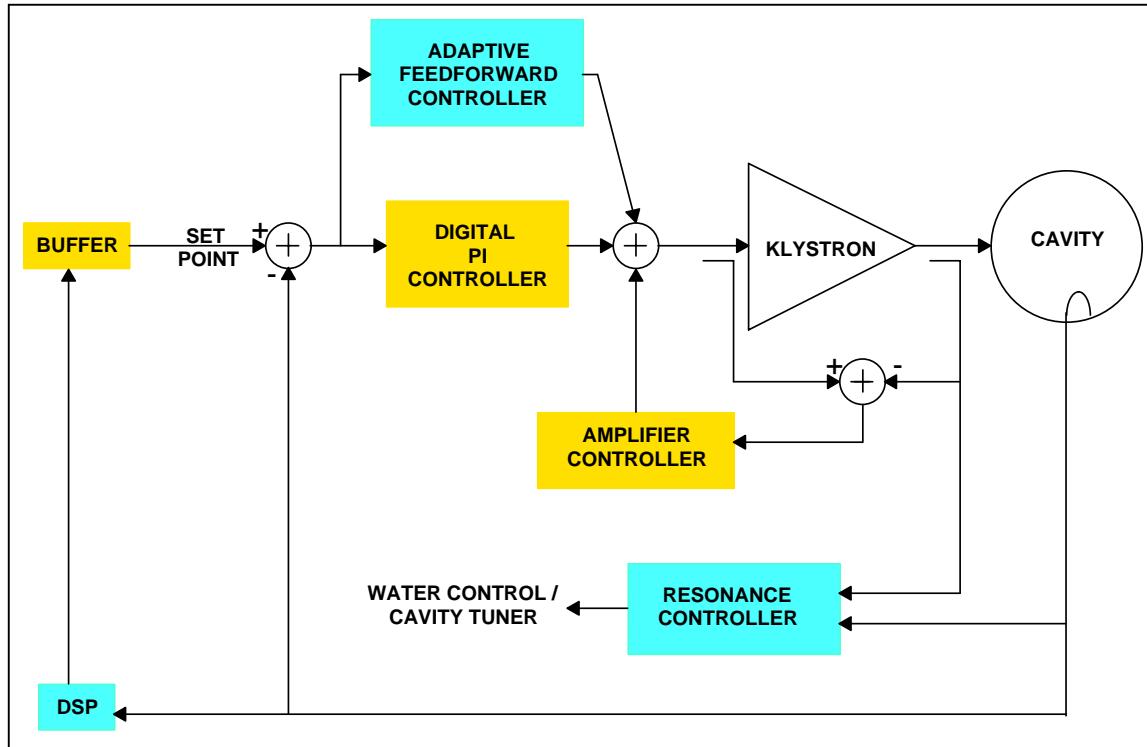
# Motherboard Production/Testing

---

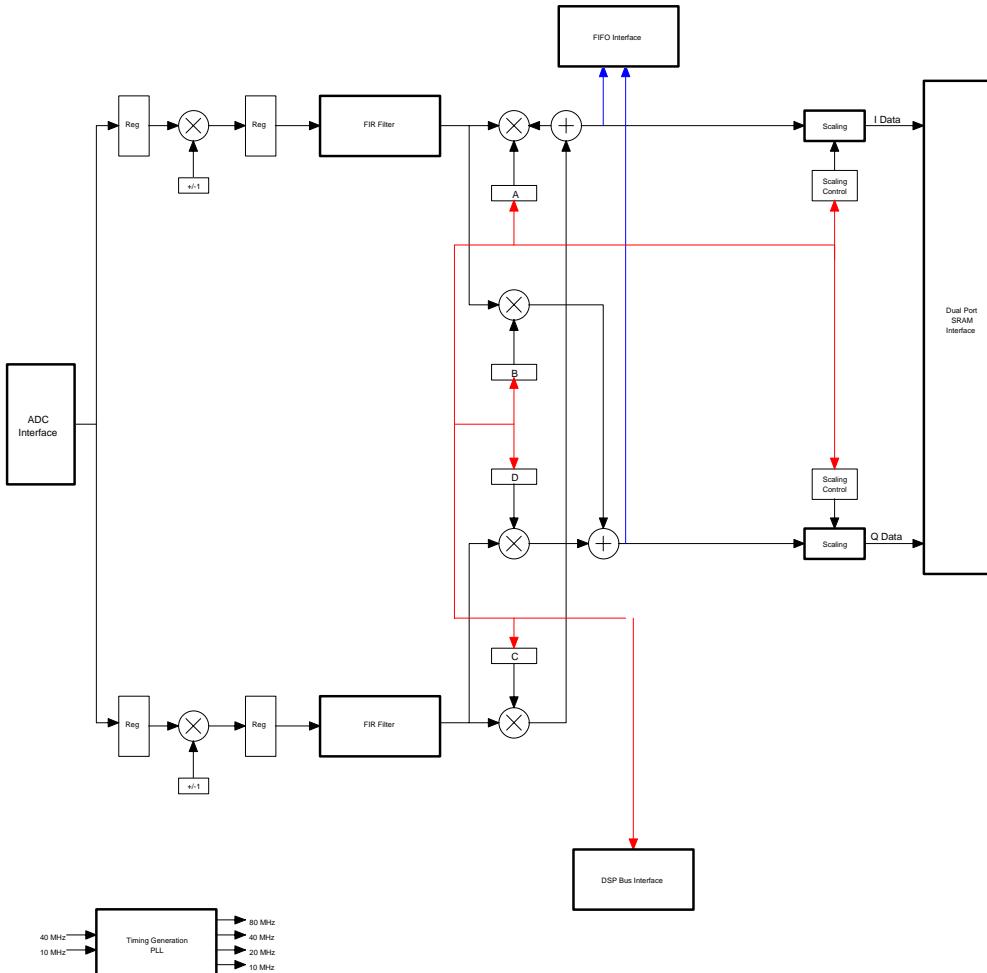


- Production
  - Common Motherboard for all configurations
  - 5 Prototype/Breadboard
  - 105 System Units
  - 10 Spares
  
- Testing
  - Using Validated VXI Interface
  - Test Control Connector
  - Test Data Connectors

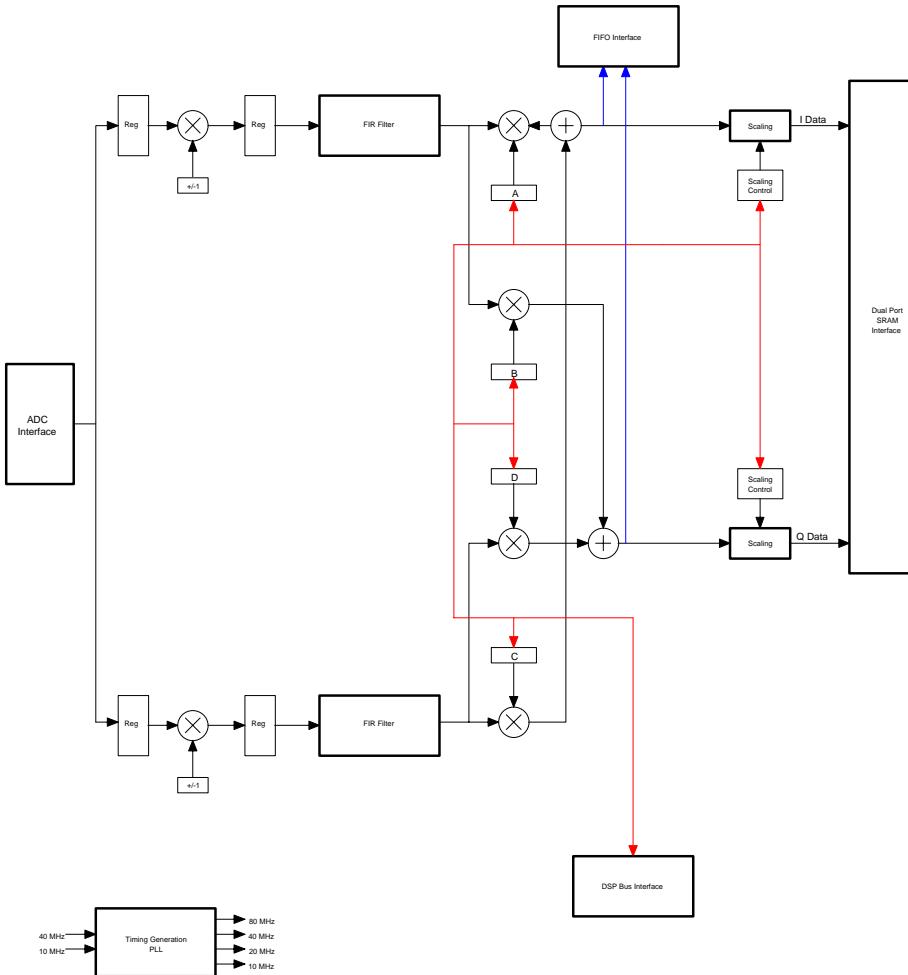
# System Block Diagram



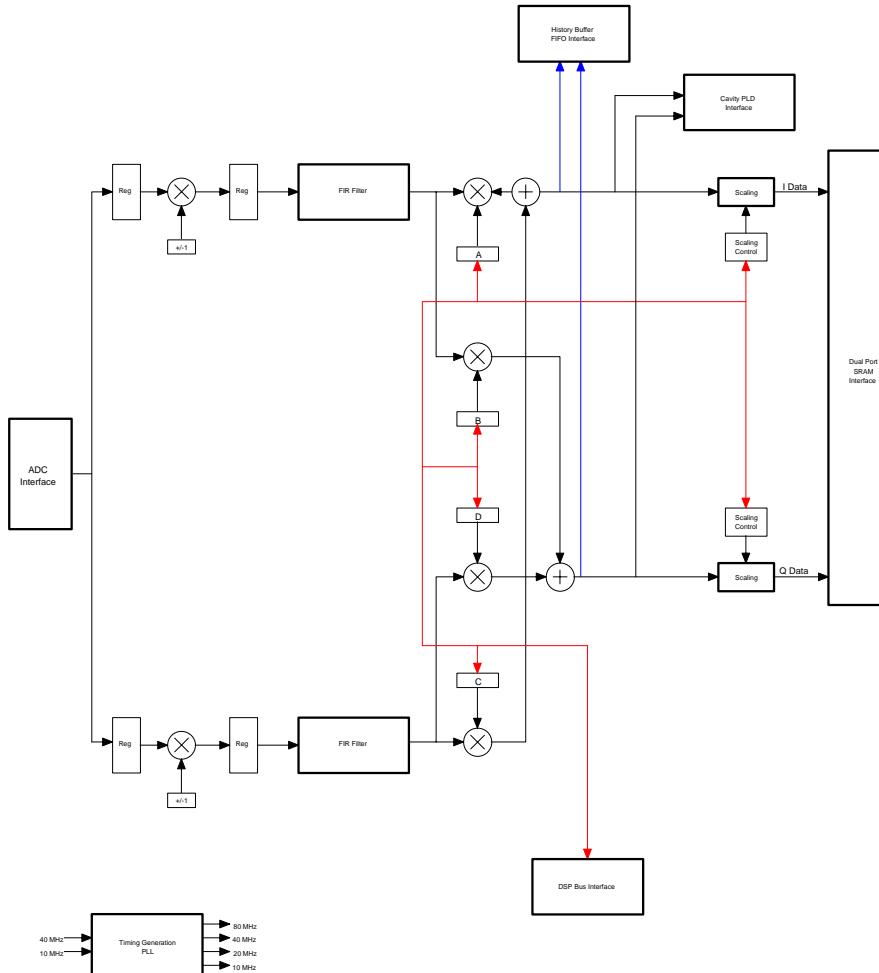
# Signal Processing – Beam Channel



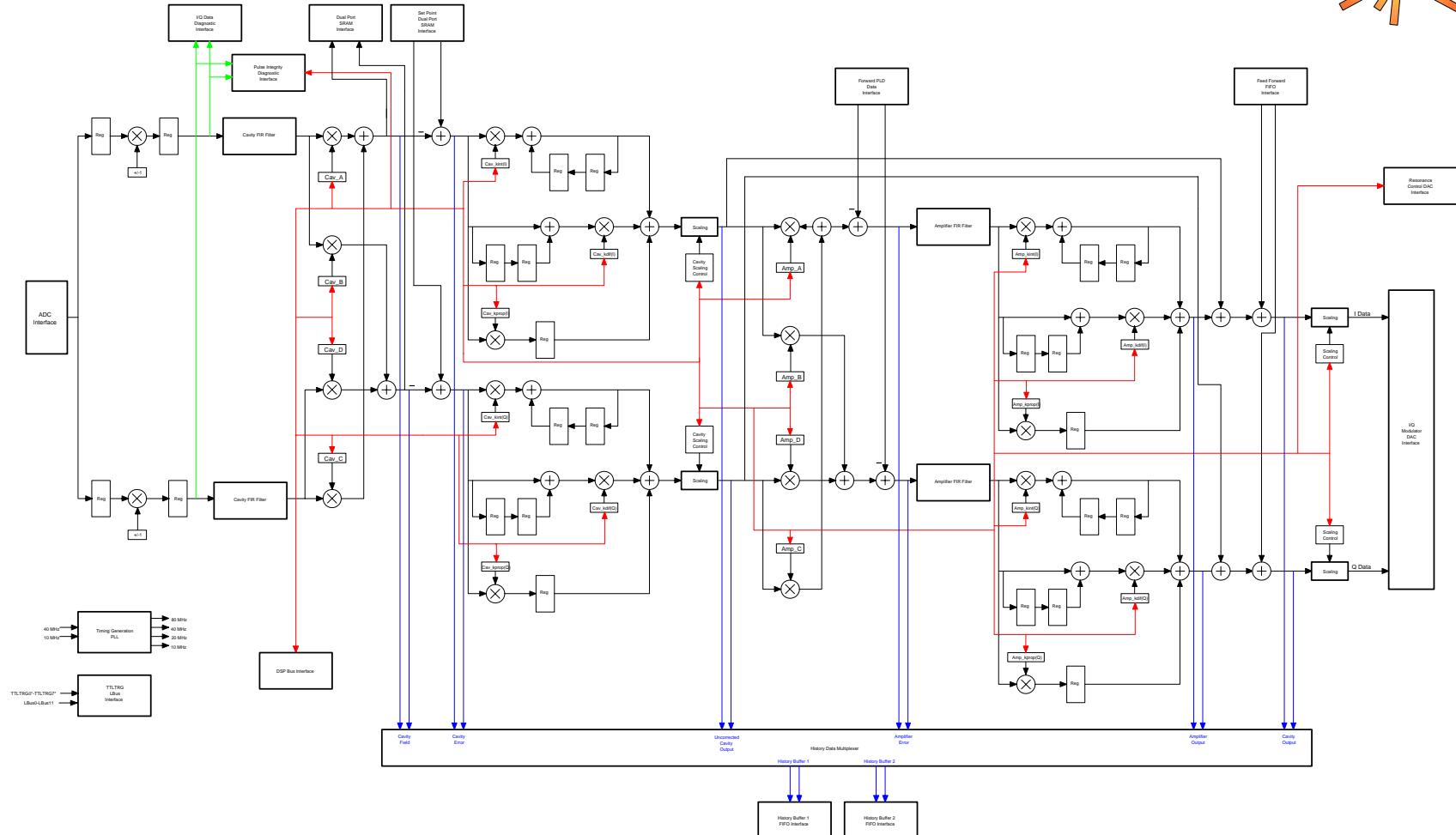
# Signal Processing – Reflected Channel



# Signal Processing – Forward Channel



# Signal Processing – Cavity Channel



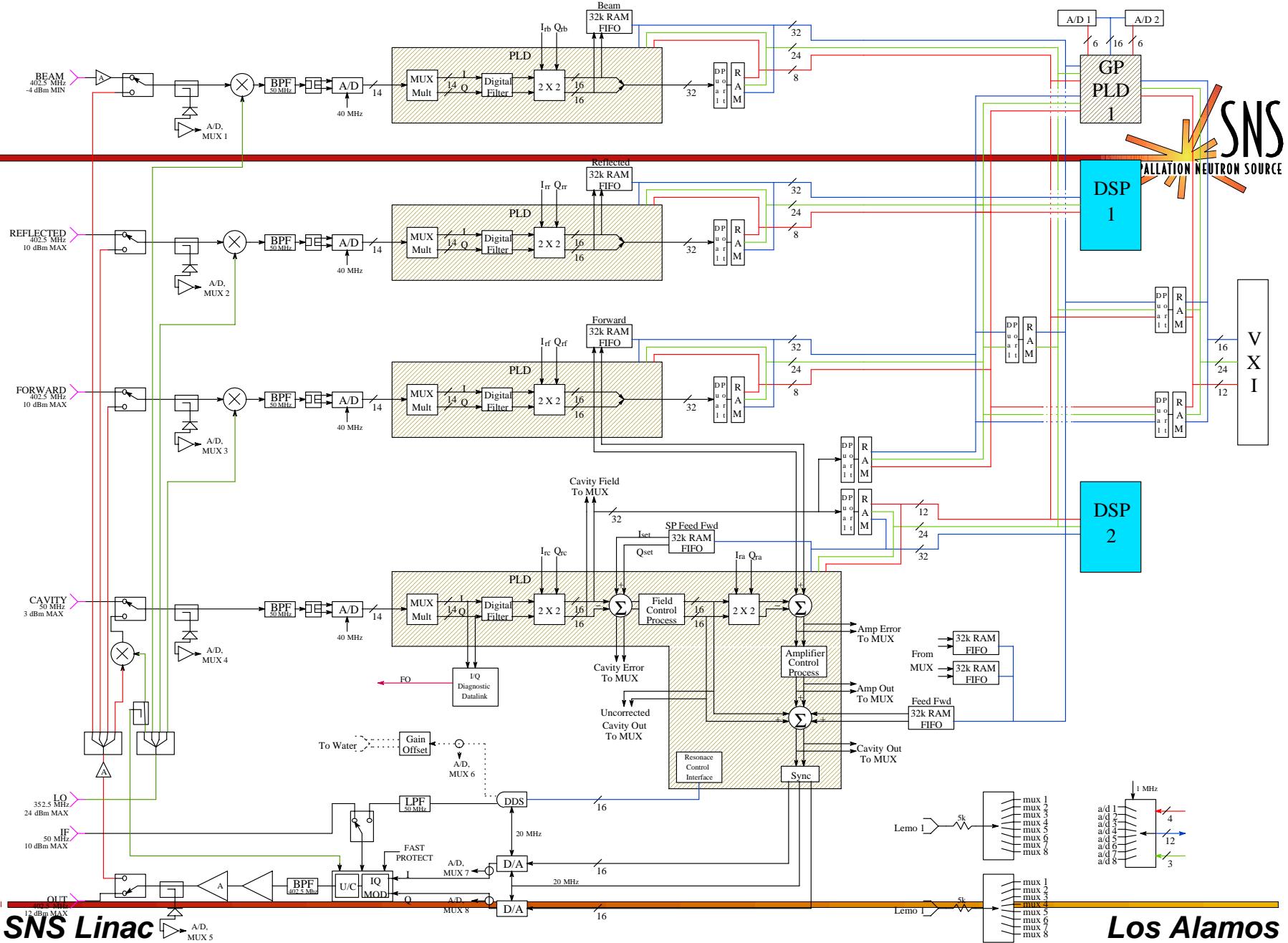
# Signal Processing - Status

---

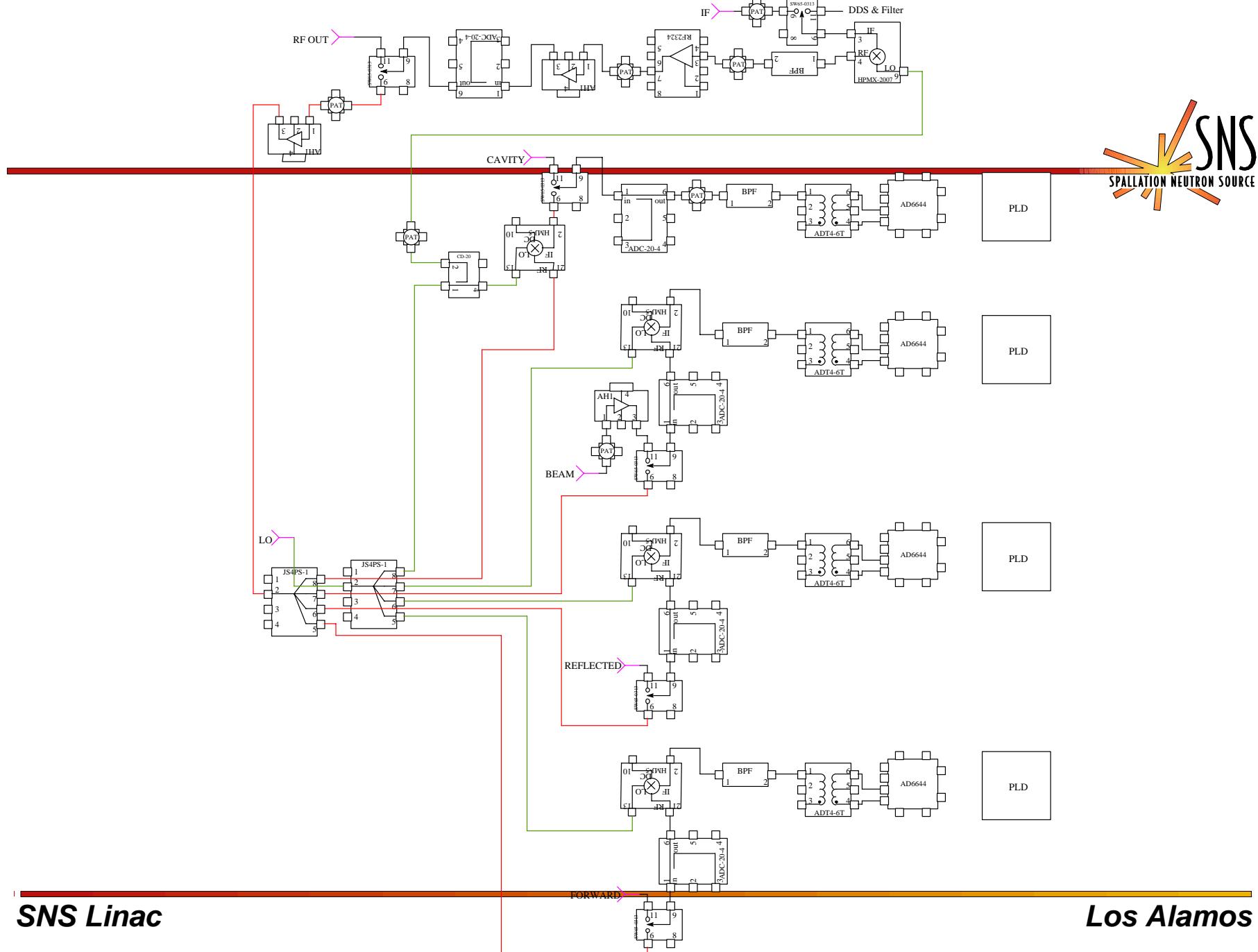


- Completing PLD Design for Pinouts
  - Cavity – 90%
  - Beam – 90 %
  - Forward – 90 %
  - Reflected – 90%
- Preparing Simulations
  - Initial functionality complete
  - Signal Path
  - Diagnostics
  - Interfaces
  - Test
- Common Design for NC and SRF

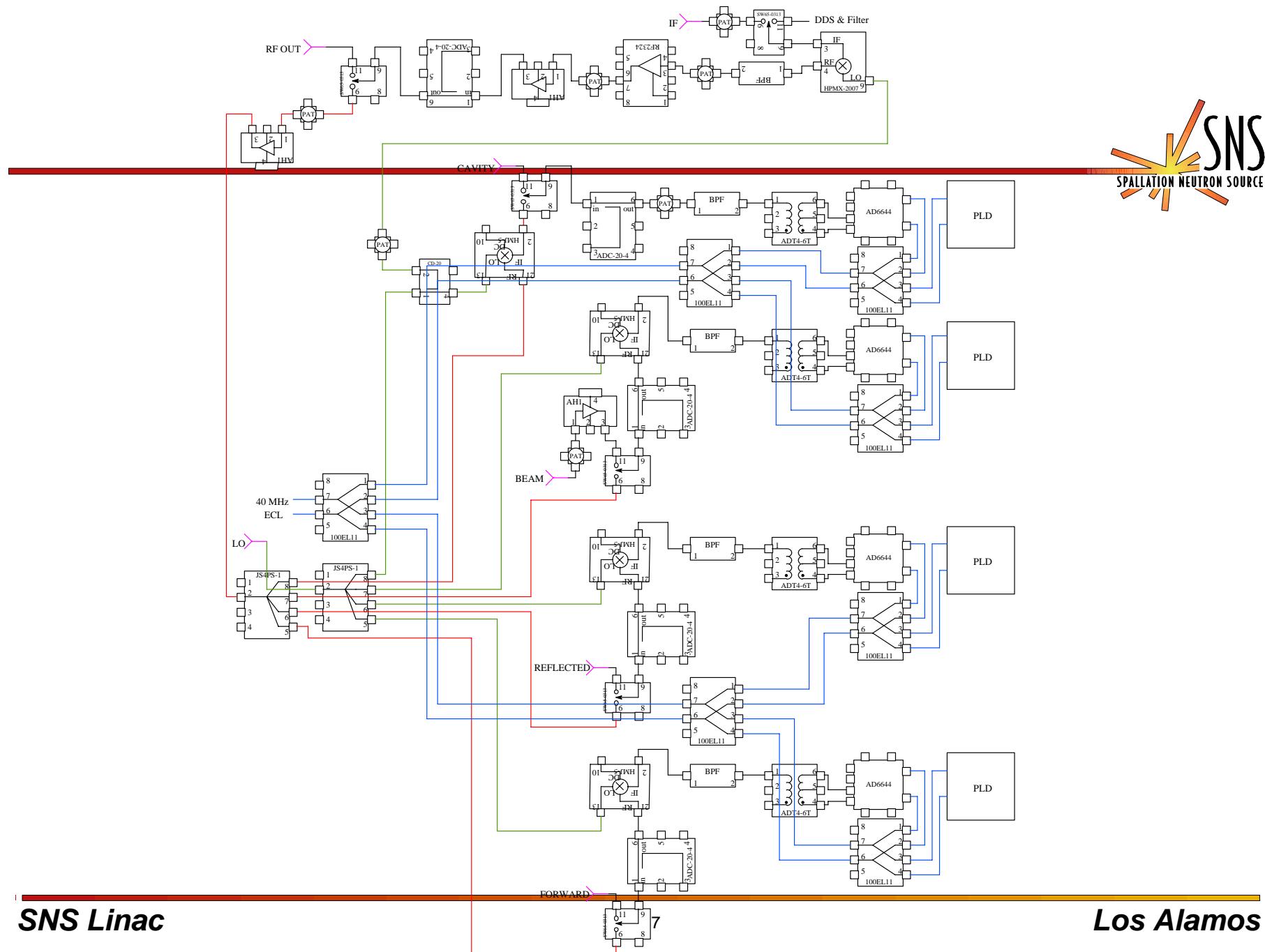
# FRCM BLOCK DIAGRAM

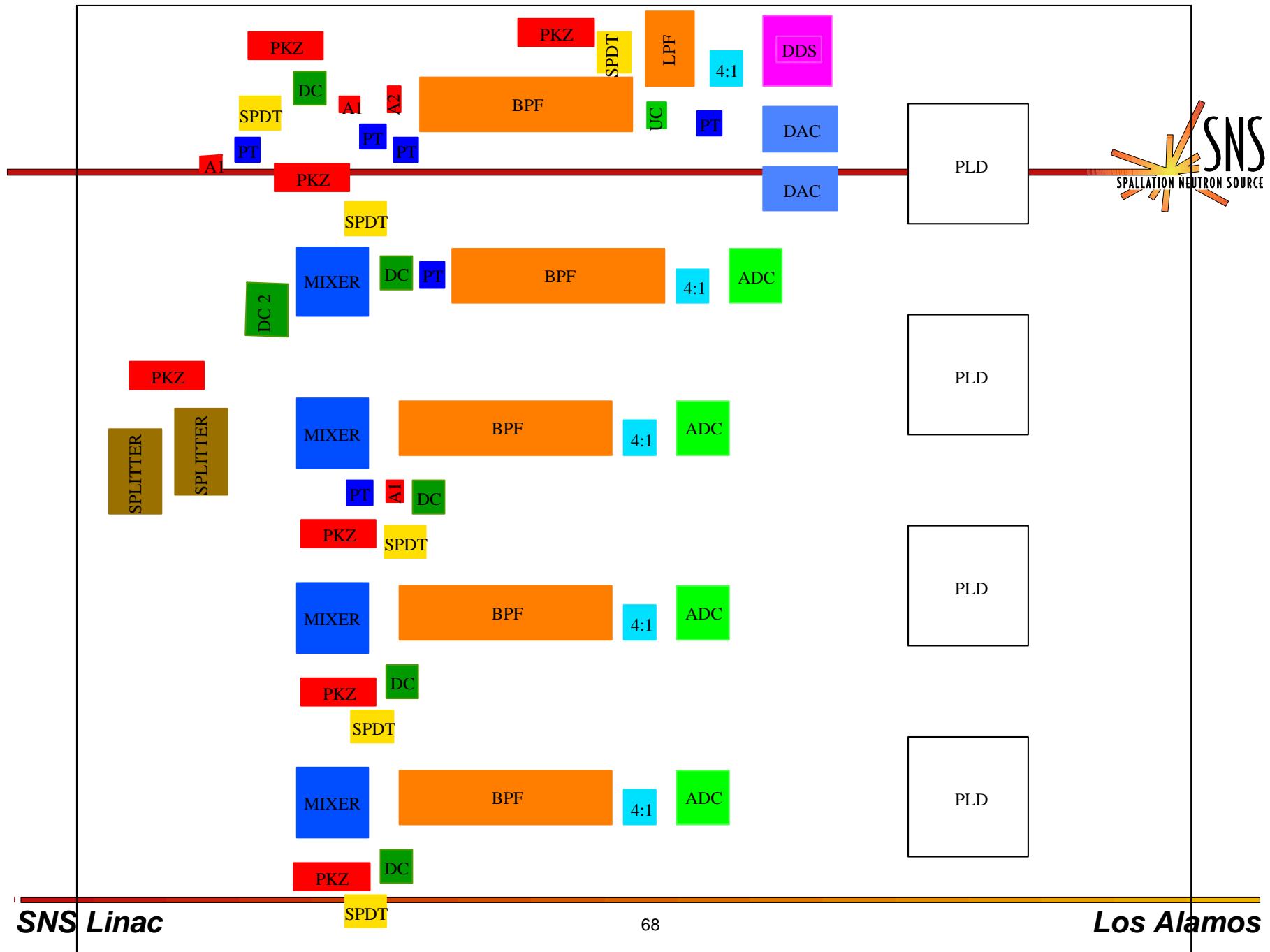


# FRCM RF LAYOUT PARTS TOP

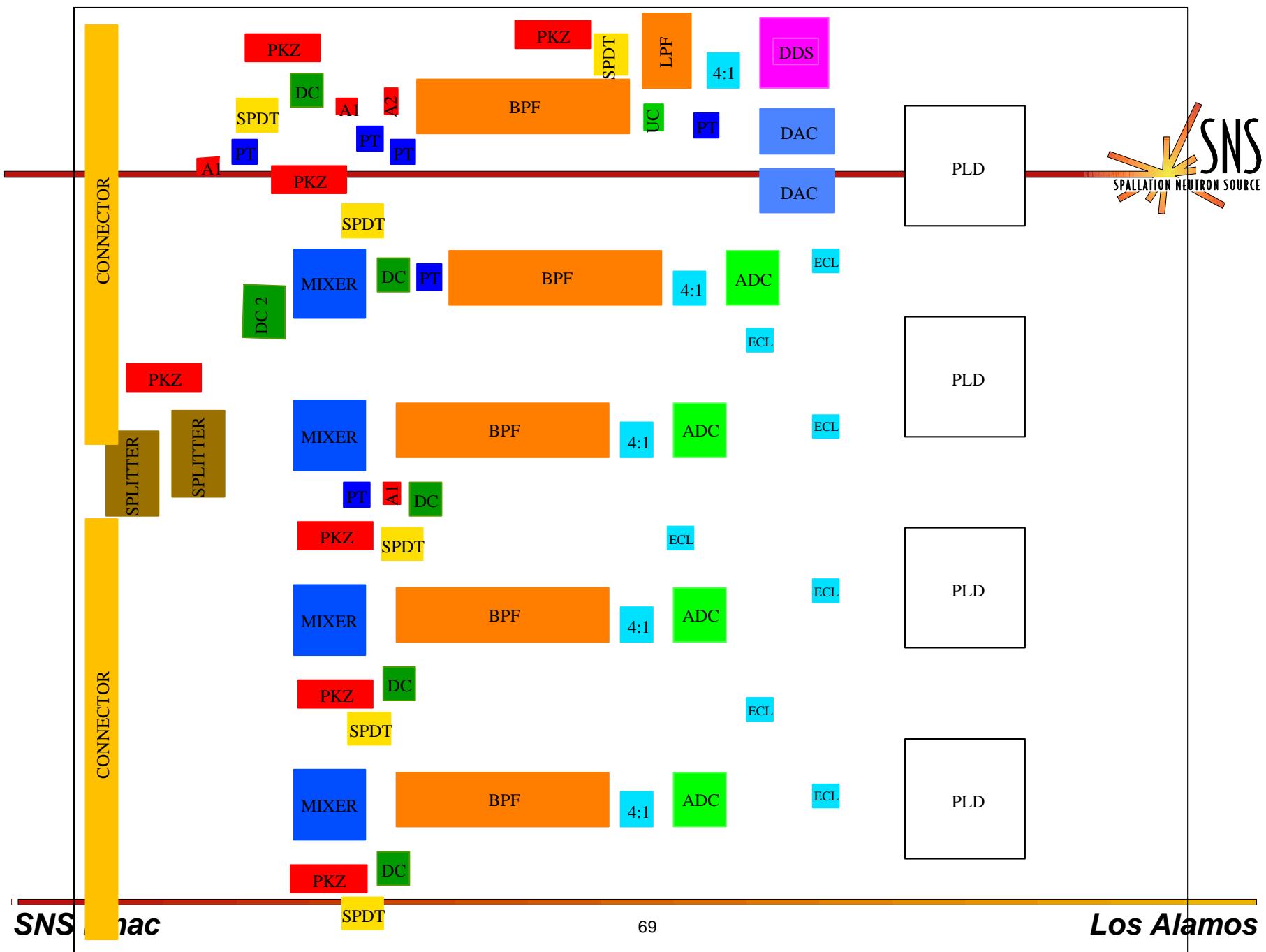


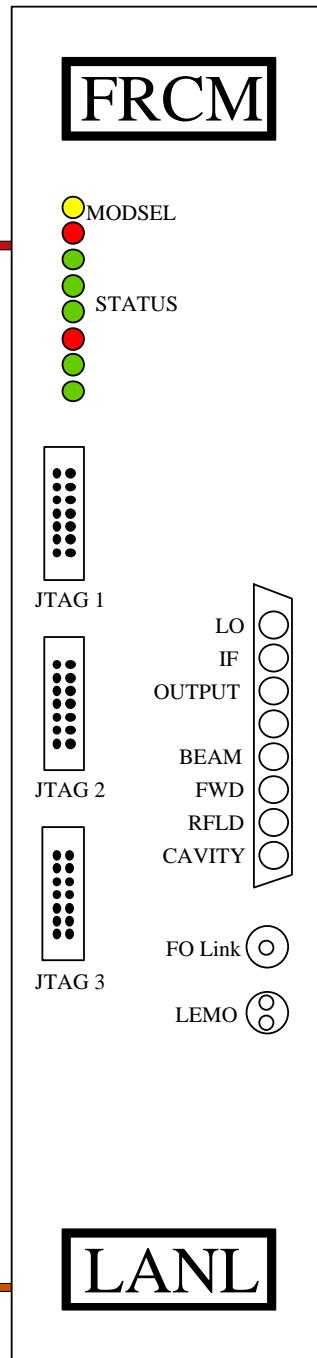
# FRCM RF LAYOUT PARTS TOP & BOTTOM





FRCM RF LAYOUT PHYSICAL TOP & BOTTOM







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# FRCM DSP DAUGHTER BOARD AND MEMORY MAP

Yi-Ming Wang  
LANL, Los Alamos, NM87544, USA

January 16, 2001

2000-0xxxx/vlb

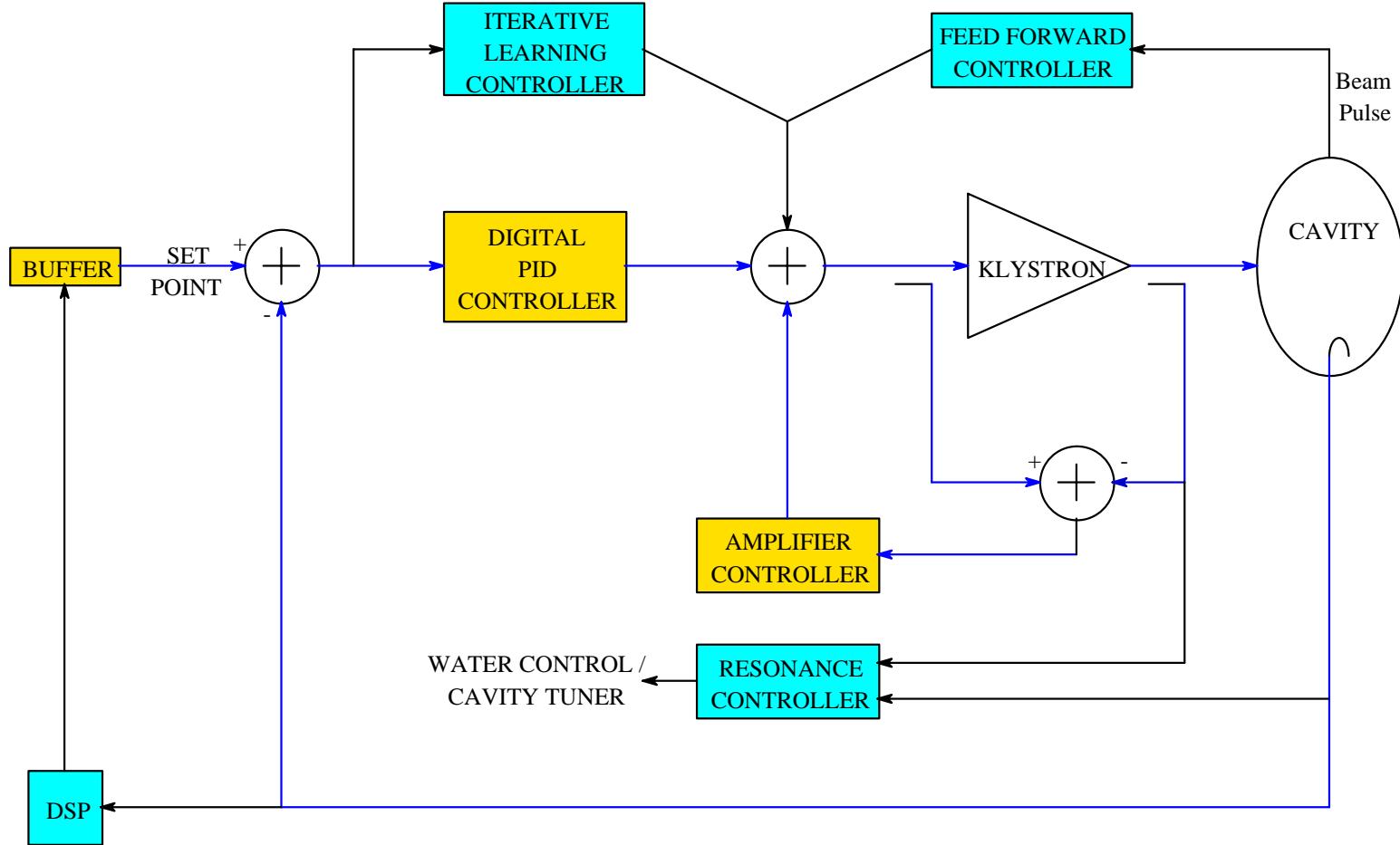
# CONTROL SYSTEM REQUIREMENTS

---

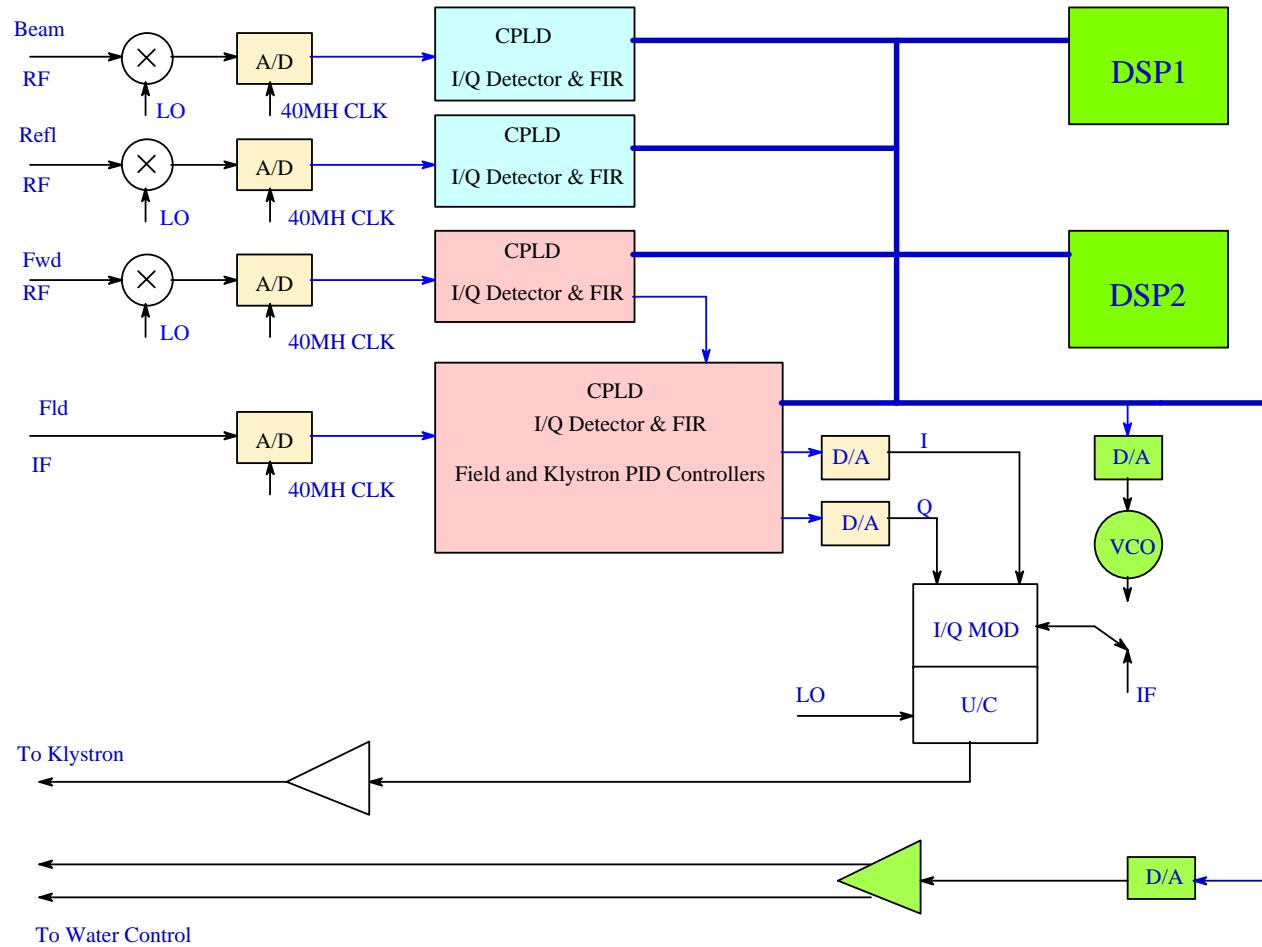


- Control Bandwidth: 200 kHz
- Latency of the signal path: <2  $\mu$ s
- Controllers: Digital PID controller and digital Feed-Forward.
- I/Q detector dynamic range: > 60dB
- I/Q detector accuracy: < .1%
- History buffers: Available along the signal paths

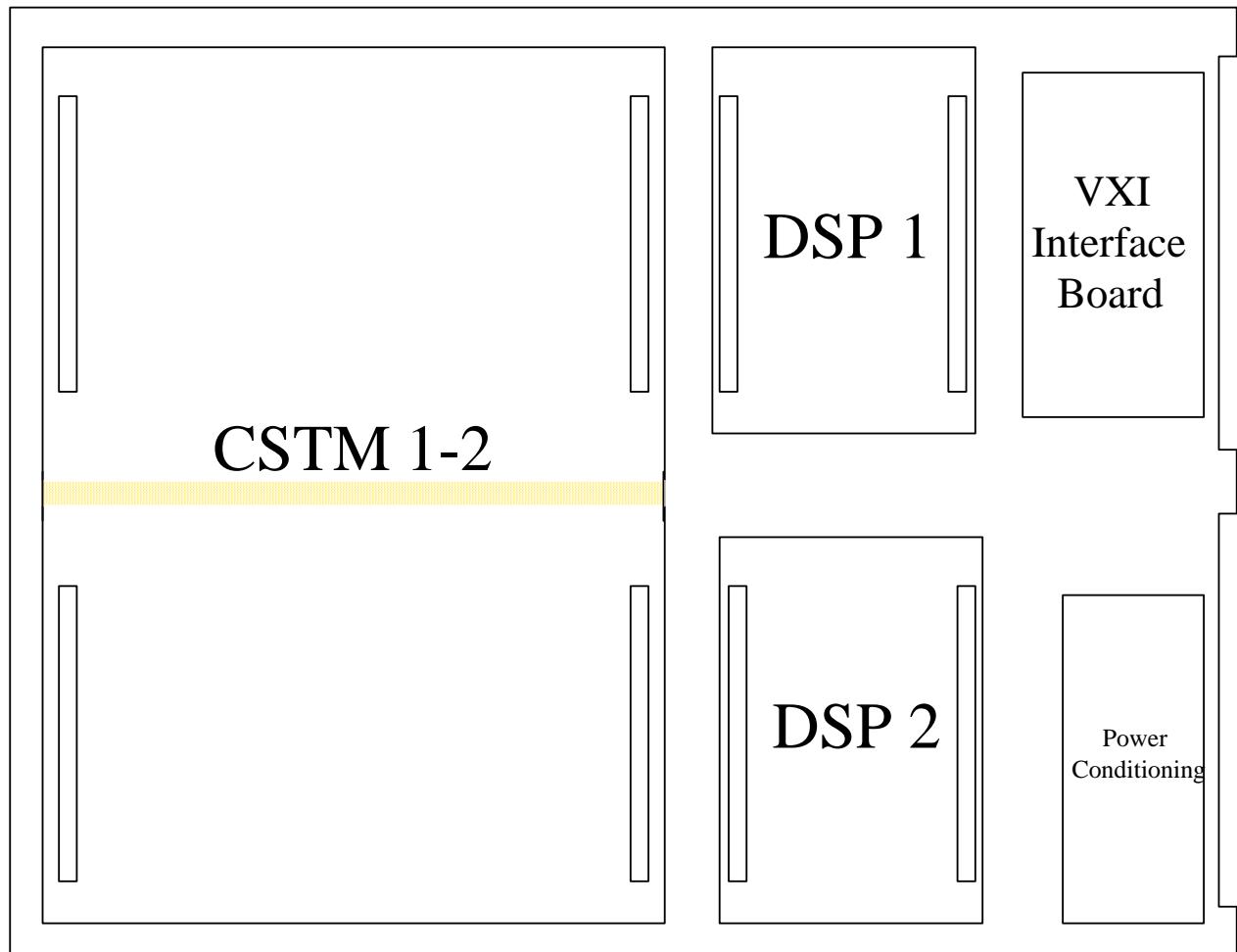
# Functional Block Diagram of the Digital Control System



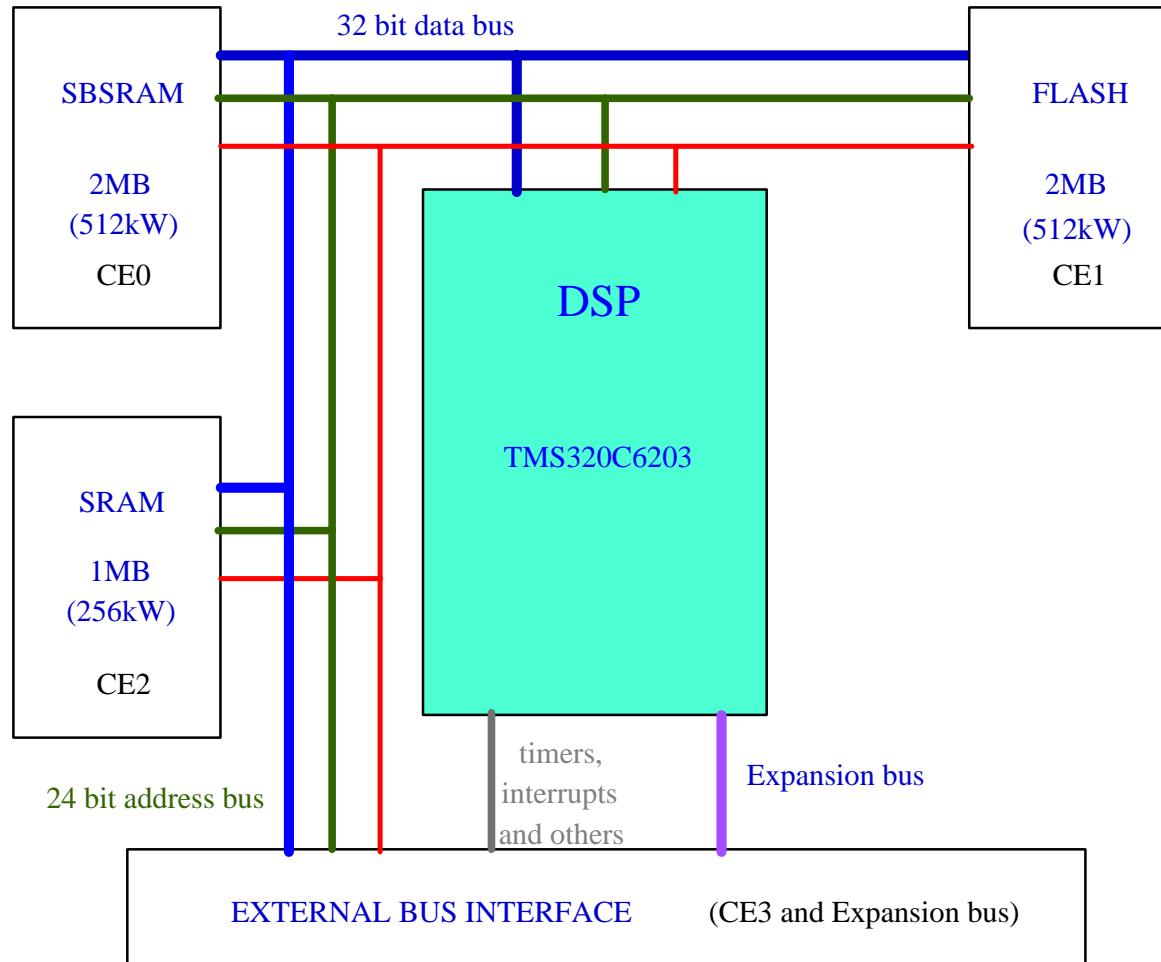
# Digital Control Module Block Diagram



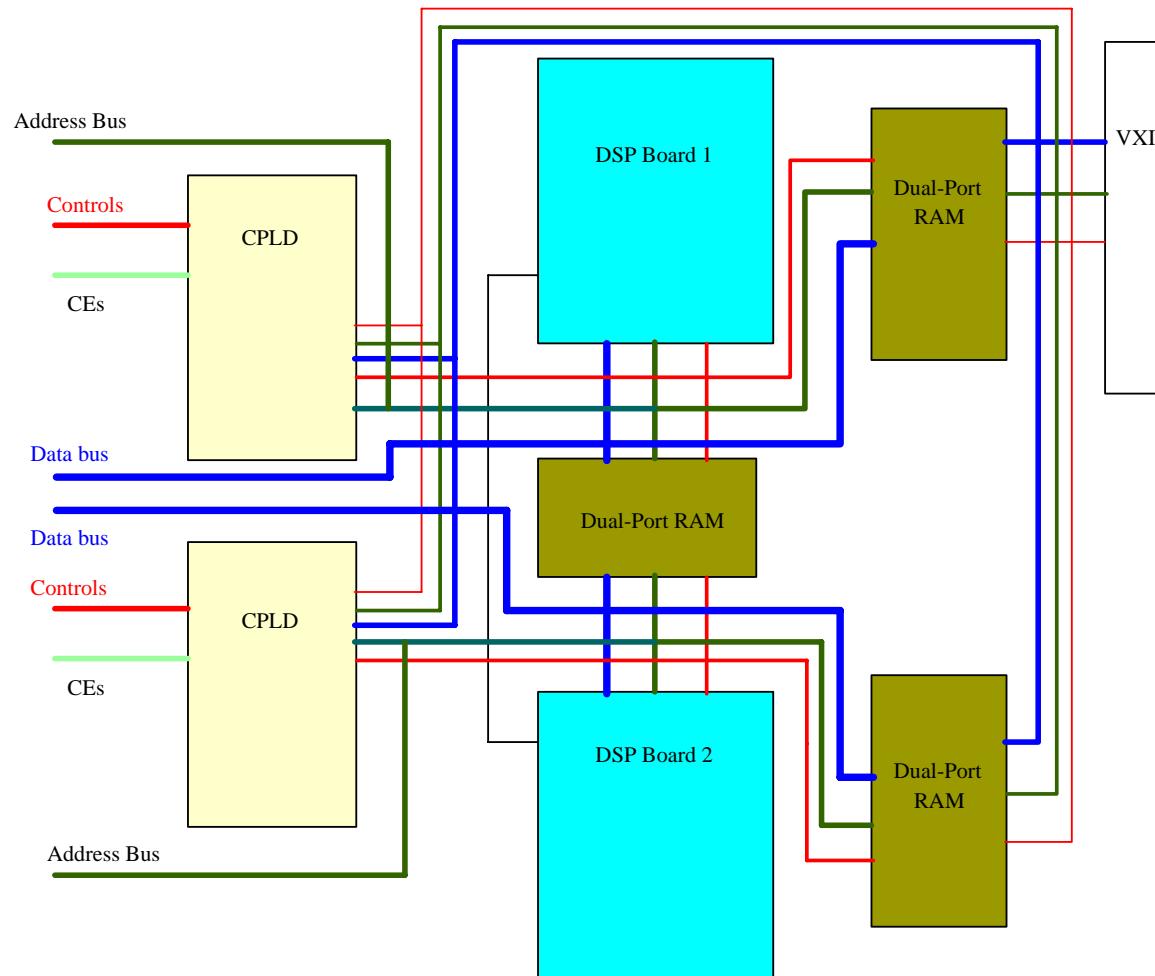
# Mother Board Layout



# DSP Board Block Diagram



# DSP Board Interfaces



# DSP ADDRESS MAP



Address Range (Hex)	Size (Bytes)	Description
0000 0000-0005 FFFF	384K	Internal Program RAM
0006 0000-003F FFFF	4M-384K	Reserved
0040 0000-005F FFFF	2M	External Memory Interface CE0 (SRAM)
0060 0000-013F FFFF	14M	CE0
0140 0000-015F FFFF	2M	External Memory Interface CE1 (FLASH)
0160 0000-017F FFFF	2M	CE1
0180 0000-01FF FFFF	8M	DSP registers and Reserved
0200 0000-02FF FFFF	16M	External memory interface CE2
0300 0000-03FF FFFF	16M	External memory interface CE3
0400 0000-3FFF FFFF	1G-64M	Reserved
4000 0000-7FFF FFFF	1G	Expansion bus XCE0-XCE3
8000 0000-8007 FFFF	512K	Internal data RAM
8008 0000-FFFF FFFF	2G-512K	Reserved

# DSP ADDRESS MAP (CE3)



Address Range	Size (Bytes)	Description
0300 0000-0300 00FF	256	Control/status registers
0300 0100-0300 FFFF	64K-256	Reserved
0301 0000-0302 FFF7	128K-8	DSP/DSP dual-port RAM
0302 FFF7	4	DSP OUT MAIL BOX
0302 FFFC	4	DSP IN MAIL BOX
0303 0000-0304 FFFF	128K	Reserved
0305 0000-0305 00FF	256	32 bit I/O ports (registers)
0305 0100-0305 FFFF	64K-256	Reserved
0306 0000-0307 FFF7	128K-8	DSP/DB dual-port RAM 0
0307 FFF8	4	DSP/DB 0 MAIL BOX
0307 FFFC	4	DB/DSP 0 MAIL BOX
0308 0000-0309 FFFF	128K	Reserved
030A 0000-030B FFF7	128K-8	DSP/DB dual-port RAM 1
030B FFF8	4	DSP/DB 1 MAIL BOX
030B FFFC	4	DB/DSP 1 MAIL BOX
030C 0000-030D FFFF	128K	Reserved
030E 0000-030F FFF7	128K-8	DSP/DB dual-port RAM 2
030F FFF8	4	DSP/DB 2 MAIL BOX
030F FFFC	4	DB/DSP 2 MAIL BOX
0310 0000-0311 FFFF	128K	Reserved
0312 0000-0313 FFF7	128K-8	DSP/DB dual-port RAM 3
0313 FFF8	4	DSP/DB 3 MAIL BOX
0313 FFFC	4	DB/DSP 3 MAIL BOX
0314 0000-0315 FFFF	128K	Reserved
0316 0000-033F FFFF	3M-384K	Reserved for DSP/DSP dual-port RAM
0340 0000-03FF FFFF	12M	Not accessible

# Part List

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- DSP: TMS320C6203GLS TI
- Flash: AM29LV800BB-70EI AMD 8 Mb(16x512K)
- SRAM: GS74116J-8 GSI 5 Mb(16x256K)
- SBSRAM: MT58L512L18PT-6 Micron 8 Mb(18x512K)

# Resonance Control (DSP#1)



- Algorithm: Using Vcav and Vfwd I/Q data (LEDA)
- Normal Operation
  - Load data from FIFO and calculation during off pulse
  - update output for each pulse
- Cavity Q measurement
  - Take measurement of the time constant of cavity
- Output: VXI control register
- Frequency Agile: DDS (IF)

# Field Control (DSP#2)

---



- Operation Mode: 8 (256kW for 8 feed forward tables)
- Update the feed-forward table 3ms before next pulse
- Operation modes are updated through VXI

# VXI INTERFACE

---



- Address space: A16/A24
- A16: Status and control registers
- A24: Dual-Port SRAM and VXI/DSP mailbox
- IRQ7 & IRQ6: DSP to VXI interrupters

# Fast Signal Processing Timing



- Inherent Filter Delay = 34 cycles (50 ns) = 1700 ns
- Processing Latency = 3.5 cycles (50 ns) = 175 ns
- Total time = 23.5 cycles (50 ns) = 1875 ns



---

# RF Controls Final Design Review

## ***SNS Linac RF Control System***

### *High Power Protection Subsystem*

Dave Thomson

**16 January 2001**

# HPPS Design Baseline



- One HPPS module (HPM) per klystron, up to two klystrons per crate (*but see Open Issues*).
- Up to 7 RF channels and up to 14 FOARC inputs per module depending on location (see table).
- Same base hardware design for all systems.
- One hardwired input (RF\_PERMIT) and one hardwired output (RF\_FAULT) plus EPICS RF\_PERMIT.
- HPM does not need to know “modes.”
- Dynamic range is more important than accuracy.
- Cavity arc algorithm will work for both NC and SRF cavities.

# HPPS Design Requirements I



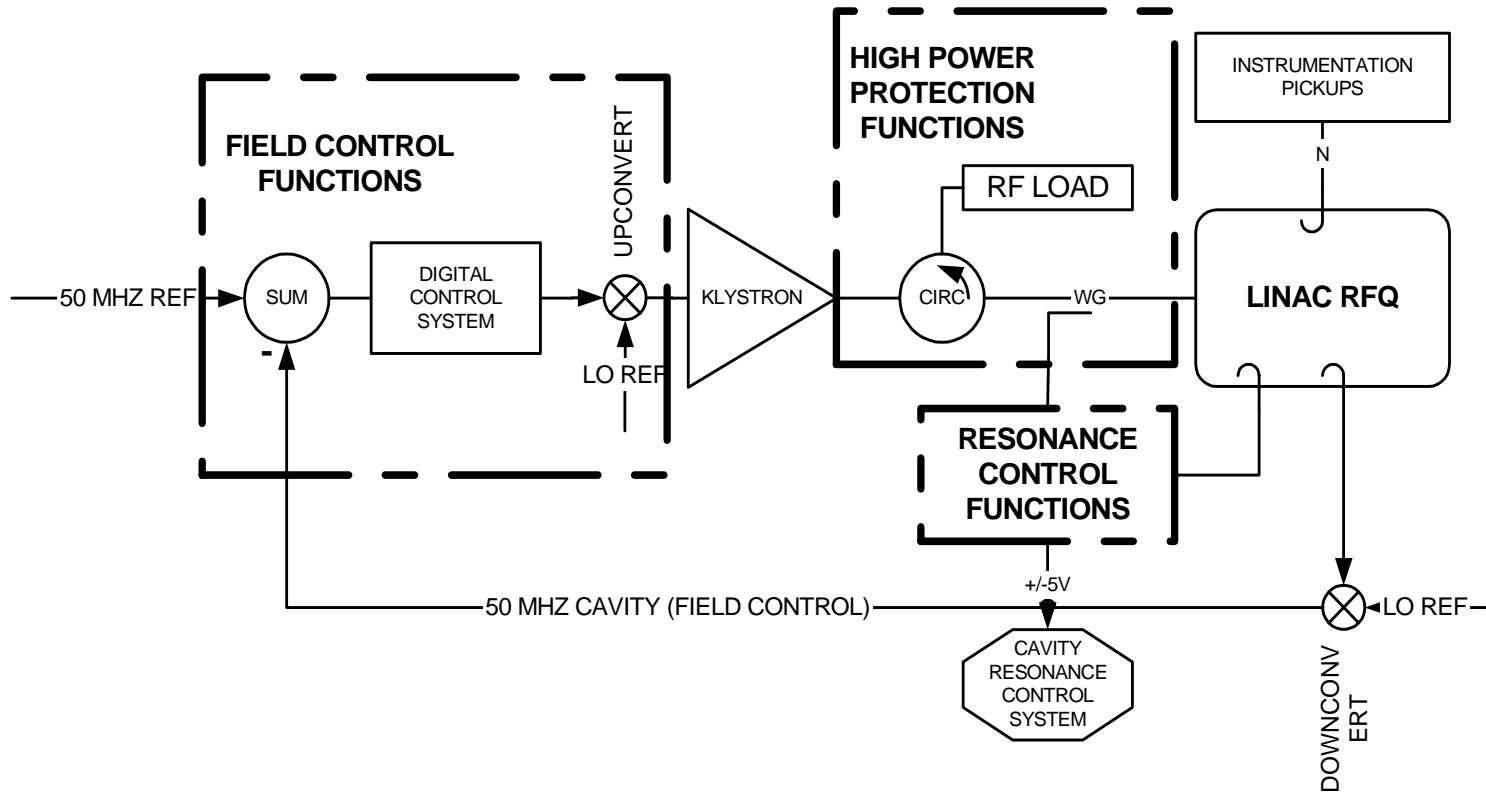
- Monitor waveguide subsystem for RF faults.
- Monitor cavity behavior for intra-cavity arcs.
- Monitor HPRF FOARC subsystem for arc faults.
- Provide opto-isolated input for RF\_PERMIT (ex *VAC\_PERMIT*).
- Provide drive to MPS opto-isolator for RF\_FAULT out.
- Provide simultaneous capture of all RF power levels on SAMPLE command (one amplitude data point per macropulse). Sample timing and control is **TBD**.

# HPPS Design Requirements II

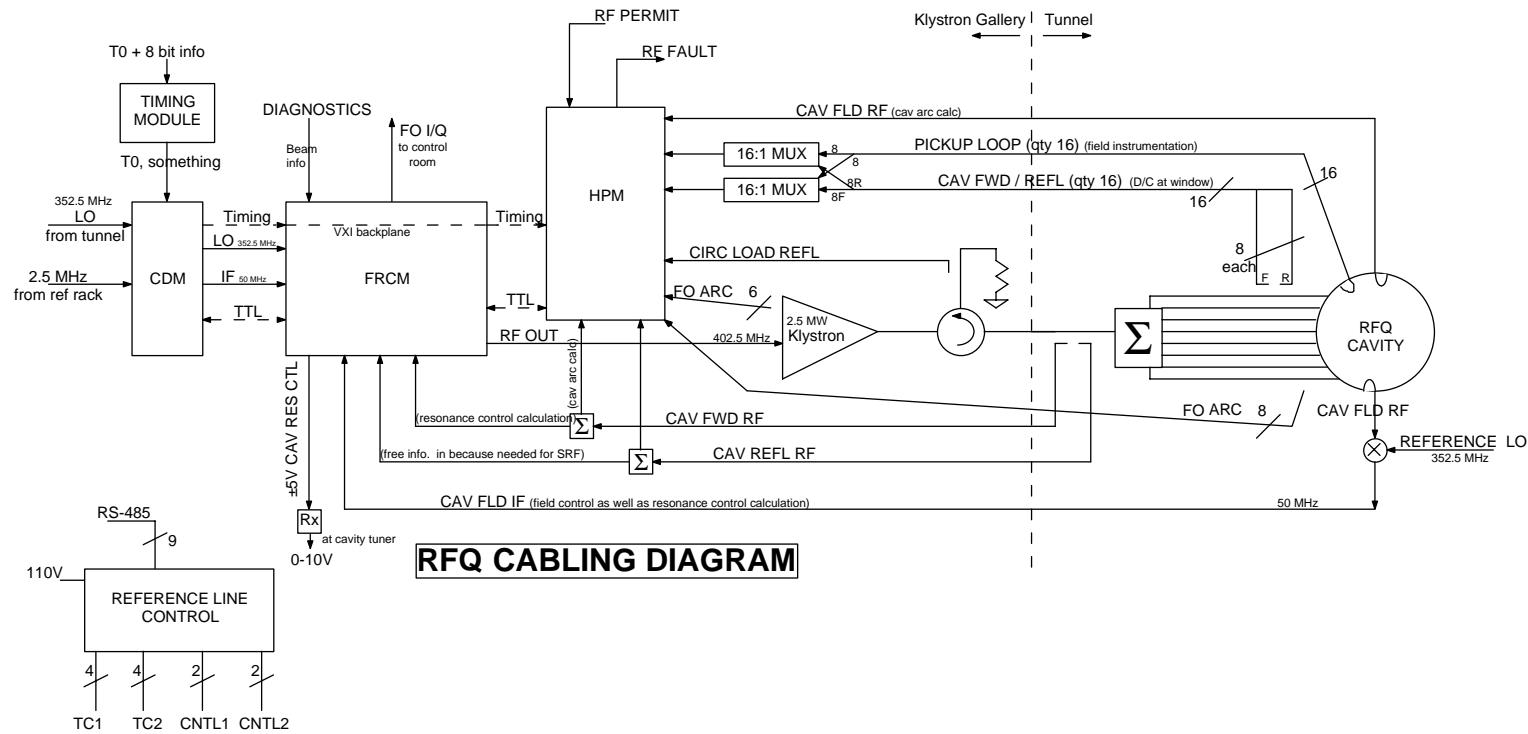


- Interface to EPICS for setting parameters and reporting status.
- Digitize 32 (16:1 x 2) multiplexed channels for RFQ segment.  
LLRF group provides the multiplexers.
- Monitor backplane fault signals in the crate and report to EPICS.
- Provide history buffers of status registers for debug.
  - Size?
- Support two klystrons/crate for SRF systems.
  - Investigate possibility of 3 RFCS systems per SRF crate.

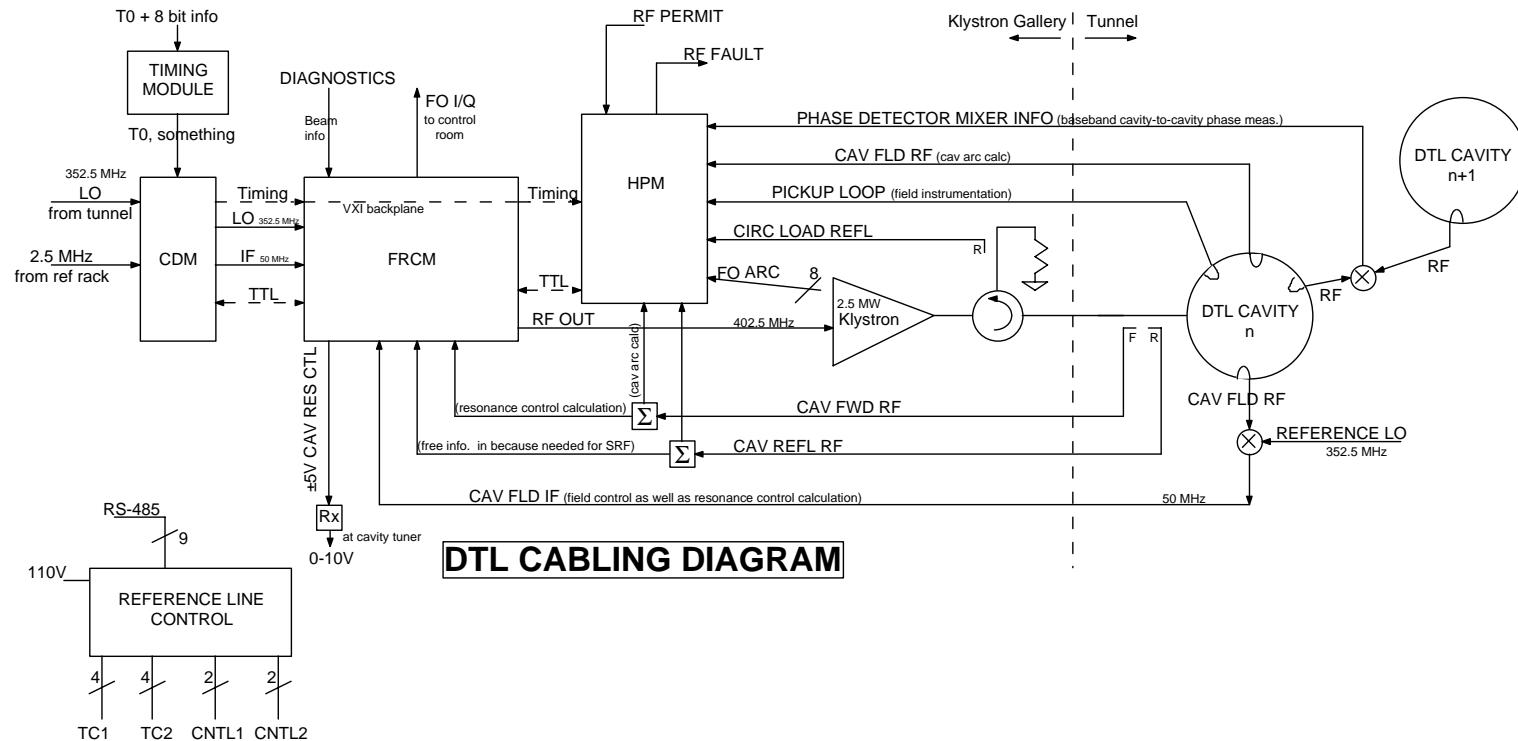
# RFCS Functional Block Diagram



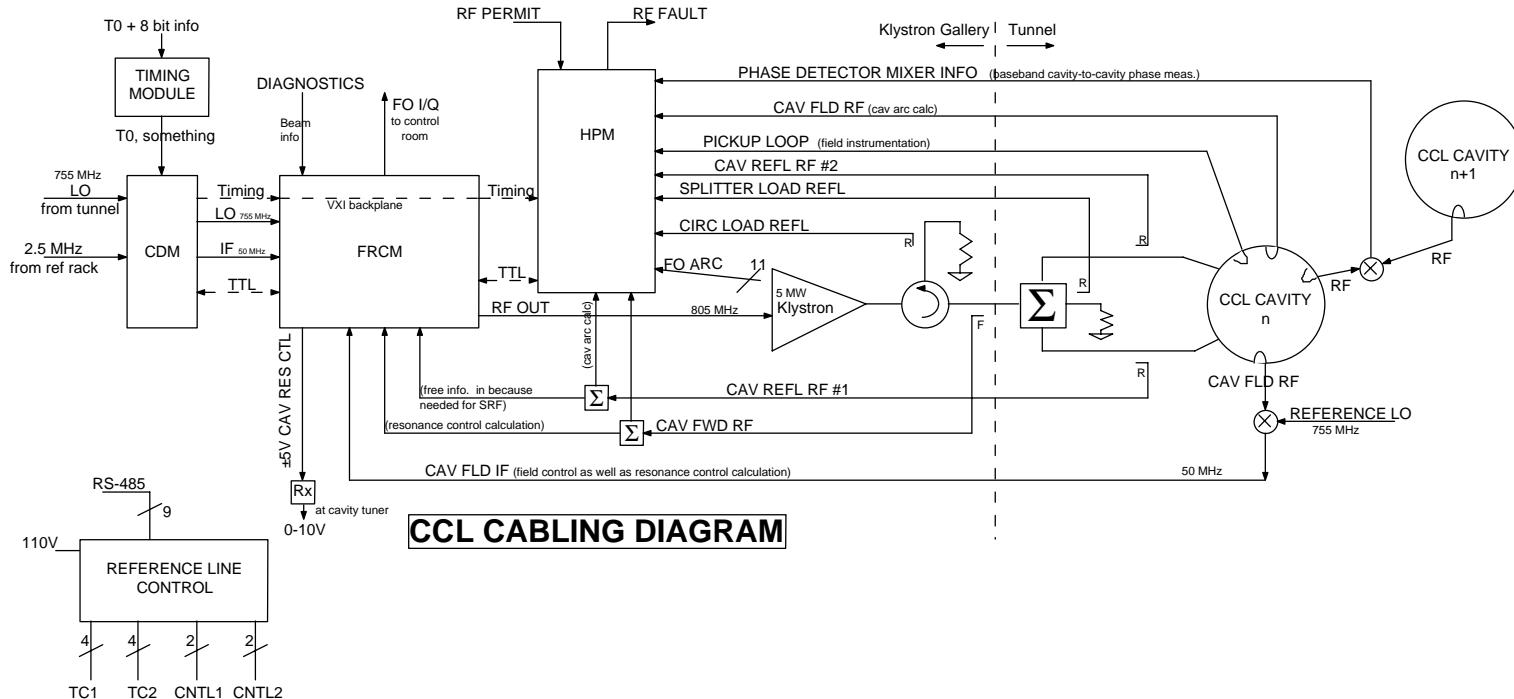
# RFQ Cabling Diagram



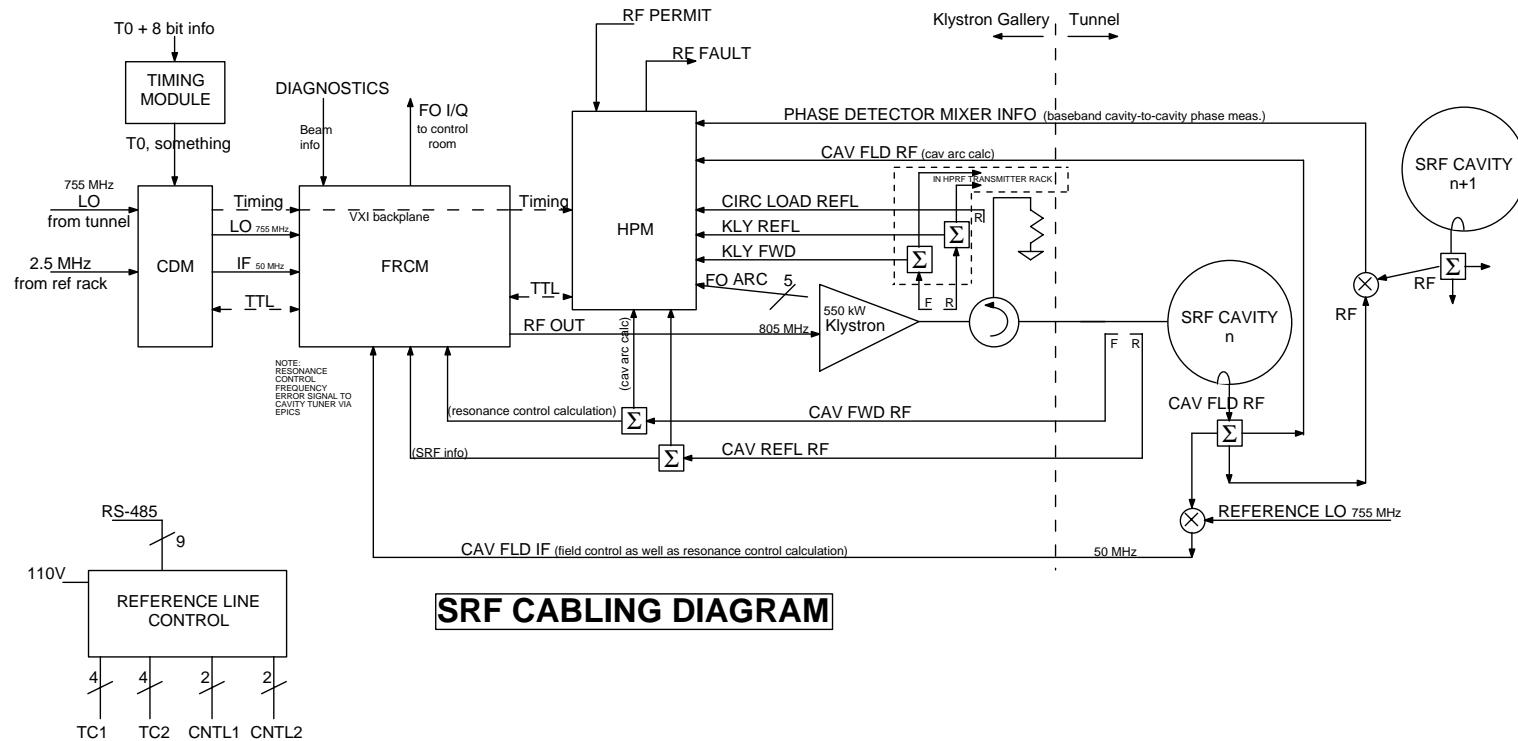
# DTL and HEBT Cabling Diagram



# CCL Cabling Diagram



# SRF Cabling Diagram



# HPPS Channel Requirements



Accelerator Stage	RF Frequency (MHz)	NC Systems	SRF Systems	Cavity Field RF + IF	Cavity RF FWD + RFL Power	Klystron FWD + RFL Power	Circulator + Splitter Load	HPM Instrument RF Channels	HPM Baseband Channel	Total RF Channels per HPM	FOARC Channels per HPM
NC RFQ	402.5	1		1 + 1	1 + 1	1 + 1	0 + 0	16:1 x 2	0	7	14
NC DTL	402.5	6		1 + 1	1 + 1	0 + 0	1 + 0	1	1	4	8
NC CCL	805	4		1 + 1	0 + 2	0 + 0	1 + 1	2	1	7	11
SRF 0.61β	805		33	1 + 1	1 + 1	0 + 0	1 + 0	0	1	3	5
SRF 0.81β	805		59	1 + 1	1 + 1	0 + 0	1 + 0	0	1	3	5
NC HEBT	805	2		1 + 1	1 + 1	0 + 0	1 + 0	1	1	4	8
Total SNS Systems		<b>13</b>	<b>92</b>								
Test Stand	402.5 & 805	1	1								
Spares	402.5	1									
Spares	805	1	6								
Total RFCS System Build		<b>16</b>	<b>99</b>								

# HPM Build Matrix



System Use	Frequency MHz	RF Channels	Total Chassis	Total RF Filters	G01 402.5 MHz 6 RF channels	G02 805 MHz 6 RF channels	G03 805 MHz 7 RF channels
Breadboard & prototypes	402.5	6	5	30	5		
RFQ	402.5	6	1	6	1		
DTL	402.5	6 (5 req'd)	6	36	6		
Spare/Test Stand	402.5	6	2	12	2		
Subtotal			14	84	<b>14</b>		
Shrinkage				<u>6</u>			
<b>Total 402.5 Filters buy</b>				<b>90</b>			
Breadboard & prototypes	805	7	5	35			5
CCL	805	7	4	28			4
SRF - Low Beta	805	6	33	198		33	
SRF - High Beta	805	6	59	354		59	
HEBT	805	6 (5 req'd)	2	12		2	
Spare/Test Stand	805	7	8	56			8
Subtotal			111	683	<b>94</b>	<b>17</b>	
Shrinkage				<u>22</u>			
<b>Total 805 Filter buy</b>				<b>705</b>			

# Fault Maturation Strategy



- Fill Time – Ignore Faults During Transients.
- Persistence – Ignore Short-Duration Faults.
- Fault Frequency Filter – Running Average Algorithm.
  - Increment a counter with every faulted macropulse. Decrement the counter with every OK pulse. If average number of faulted pulses exceeds average number of OK pulses, counter overflows and latches off the system (requires operator reset). The averaging time is set by the counter overflow value and the pulse repetition rate.

# Fault Actions

---



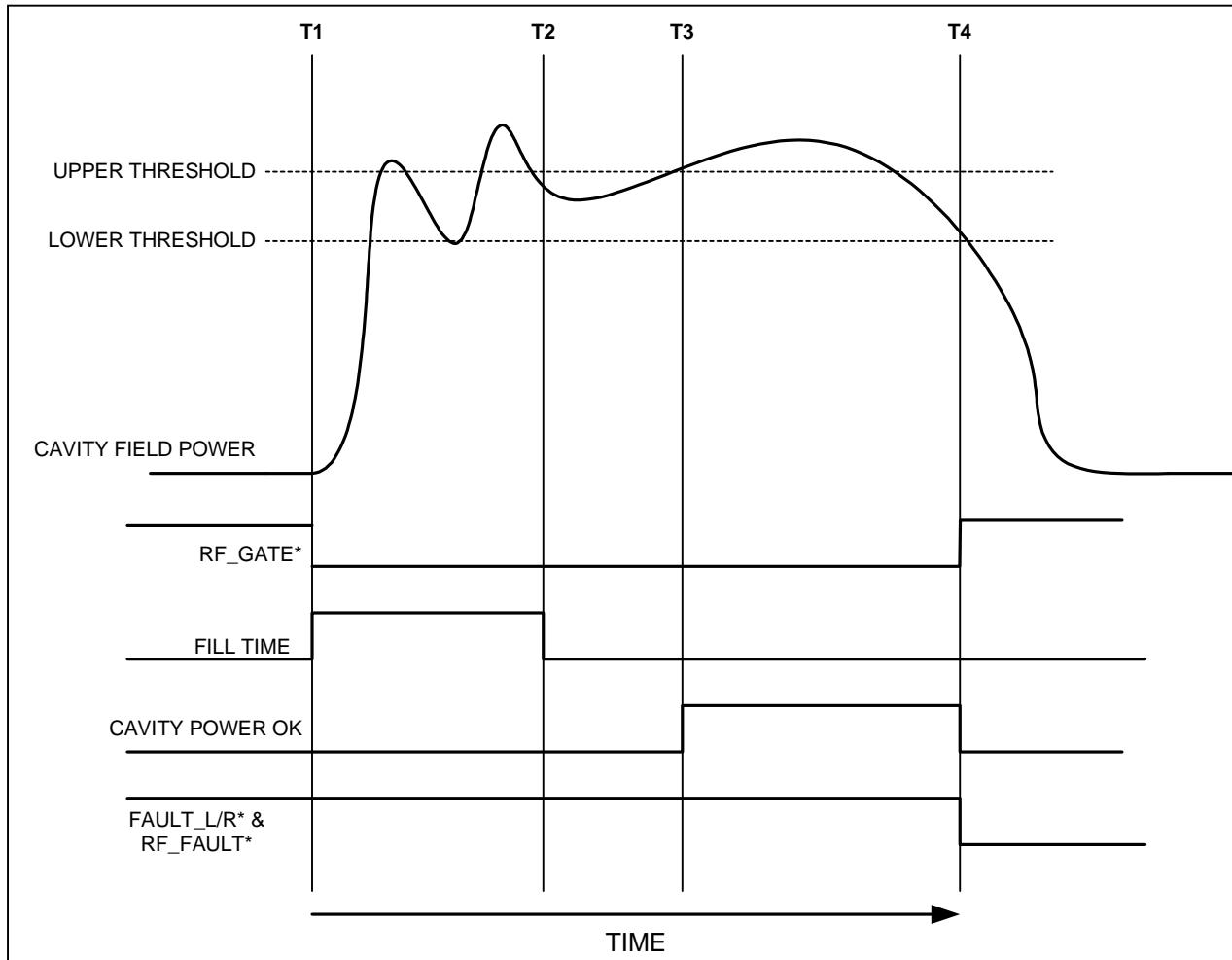
- Blank RF carrier to end of macropulse if:
  - Power is over threshold on RF loads (load fault).
  - Power is over threshold on cavity reflected power.
  - Cavity arc is detected (see slide).
  - FOARC is detected.
  - RF\_PERMIT *hardware* input faults. (Vacuum?)
  - RF\_PERMIT *software* input faults (EPICS).
  - Fault asserted on VXIbus backplane by other LLRF modules associated with *the same klystron*.
- Assert RF\_FAULT output to MPS.
- Do not release RF\_FAULT until fault clears.

# FOARC Functions

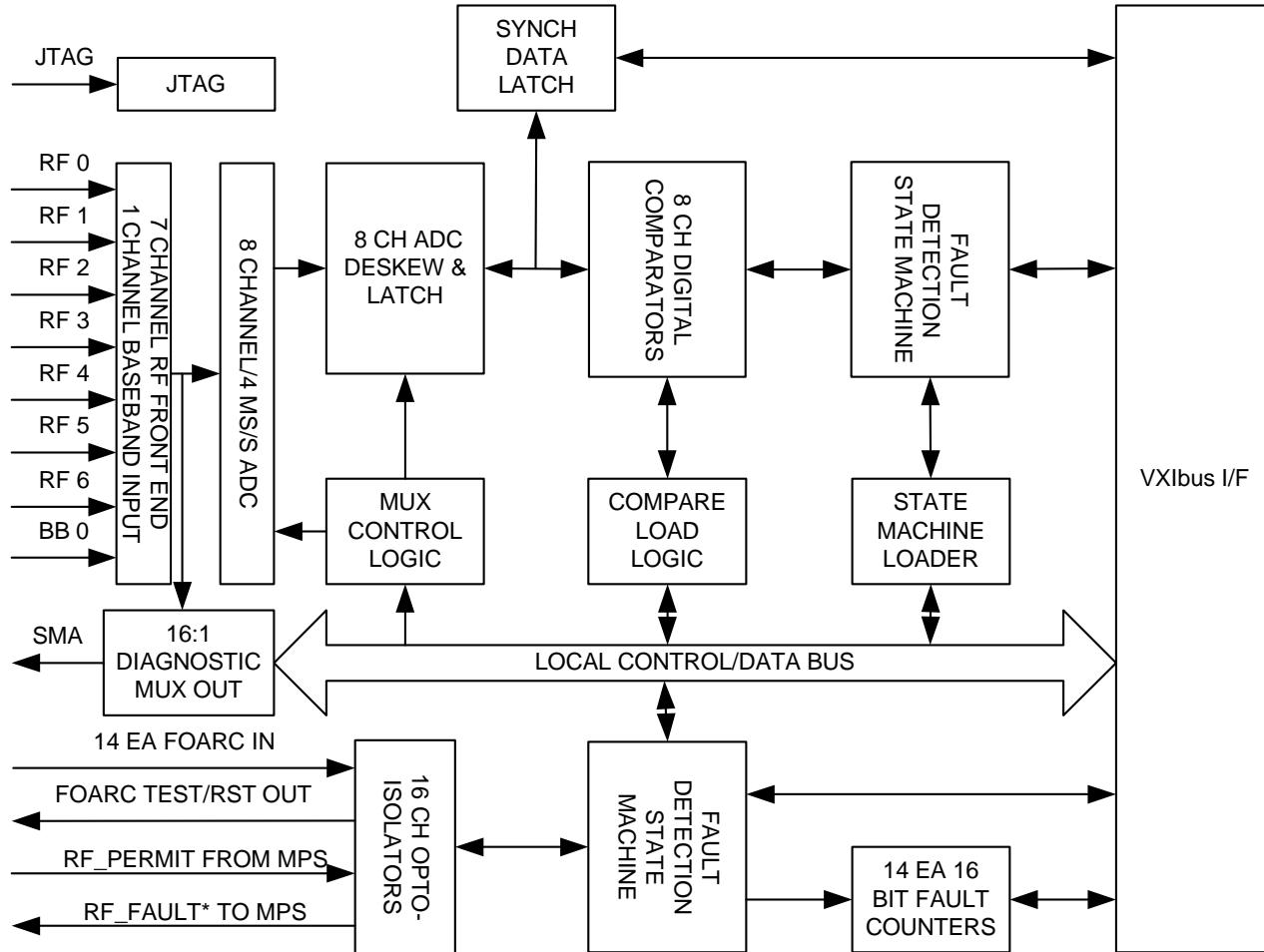


- FOARCs are detected by the High Power RF group and signaled to HPM via opto-isolated control lines.
- Any FOARC event results in blanking the RF to the end of the macropulse.
- Repetitive FOARCs will trigger the fault frequency algorithm, latching off the system.
- HPM provides built-in-test of FOARC – AFT interface.
- 16-Bit counters monitor FOARC channel activity.
- Unused FOARC channels are maskable.
- Upper 4 channels can be used for auxiliary opto-isolated binary inputs per ORNL request.

# RF Cavity Arc Detection Strategy



# HPM Block Diagram



# Analog Signal Processing

---



- Analog Signal Acquisition:
  - Seven RF channels, one baseband analog channel.
  - 4 Ms/s 10 bit 8 channel ADC (Zilog XRD 6418).
  - 2  $\mu$ s ADC update rate with  $\sim$  2.5  $\mu$ s pipeline delay.
  - Total response time  $\sim$  5  $\mu$ s.
- Narrow band input filter ( $\sim$  20 MHz) at  $F_0$  with log video detector (AD8313). No phase information.
- RF Dynamic Range  $\sim$  62 dB (5 MW – 3 W).
- No overload protection/limiting – signals scaled for max fault at +10.0 dBm at front panel connector.
- Digital level comparators – no DACs like on LEDA.

# Calibrations and Accuracy

---



- Only the RF channels are calibrated.
- The baseband channel is used for indication only.
  - Sign of the baseband signal is not important.
- Each RF detector channel has zero and span pots for calibration.
  - Zero takes out the output offset of the detector.
  - Full scale is set to +4.95 VDC with +10.0 dBm at the front panel connector.
- The ADC provides an overflow signal if the input exceeds the +5.00 V reference.
- Analog channels are auto-zeroed on every pulse.

# RF Accuracy



- RF pads used to normalize input filter insertion loss. Pad value based on filter vendor test data to scale input to RF detector to  $-2 \text{ dBm}$  with  $+10 \text{ dBm}$  input. Filter passband ripple less than  $\pm 0.1 \text{ dB}$ .
- Acquisition Accuracy:
  - Detector sensitivity:  $80 \text{ mV/dB}$ .
  - ADC:  $4.95\text{V FS}/1024 = 4.84 \text{ mV/bit}$ .
    - $V_{ref}: \pm 2 \text{ mV} \pm 5 \text{ ppm}/^\circ\text{C} \times 20 \text{ }^\circ\text{C} = \pm 2.5 \text{ mV}$ .
    - $DNL (\pm 1 \text{ LSB}) + INL (\pm 2 \text{ LSB}) = \pm 3 \text{ bits}$ .
    - $3 \text{ bits} \times 4.84 \text{ mV/bit} + 2.5 \text{ mV } V_{ref} = \pm 17 \text{ mV}$ .
- Acquisition Uncertainty:  $17 \text{ mV}/80 \text{ mV/dB} = \pm 0.2 \text{ dB}$ .
- **Total uncertainty approximately  $\pm 0.3 \text{ dB}$ .**

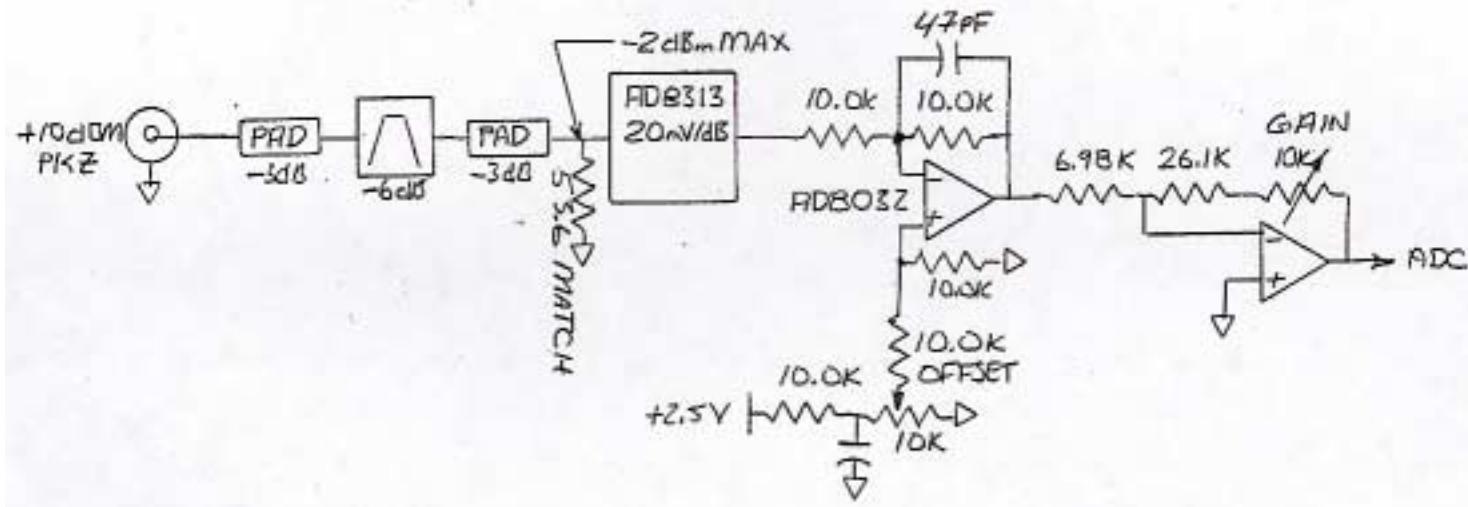
# Digital Functions

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- PLD Logic decode/actions for speed.
- Parameters set/read *via* EPICS.
- Housekeeping:
  - Power supply monitors
  - Clock monitors
  - Front panel LEDs

# RF Front End



# AD8313 Response at 100 MHz

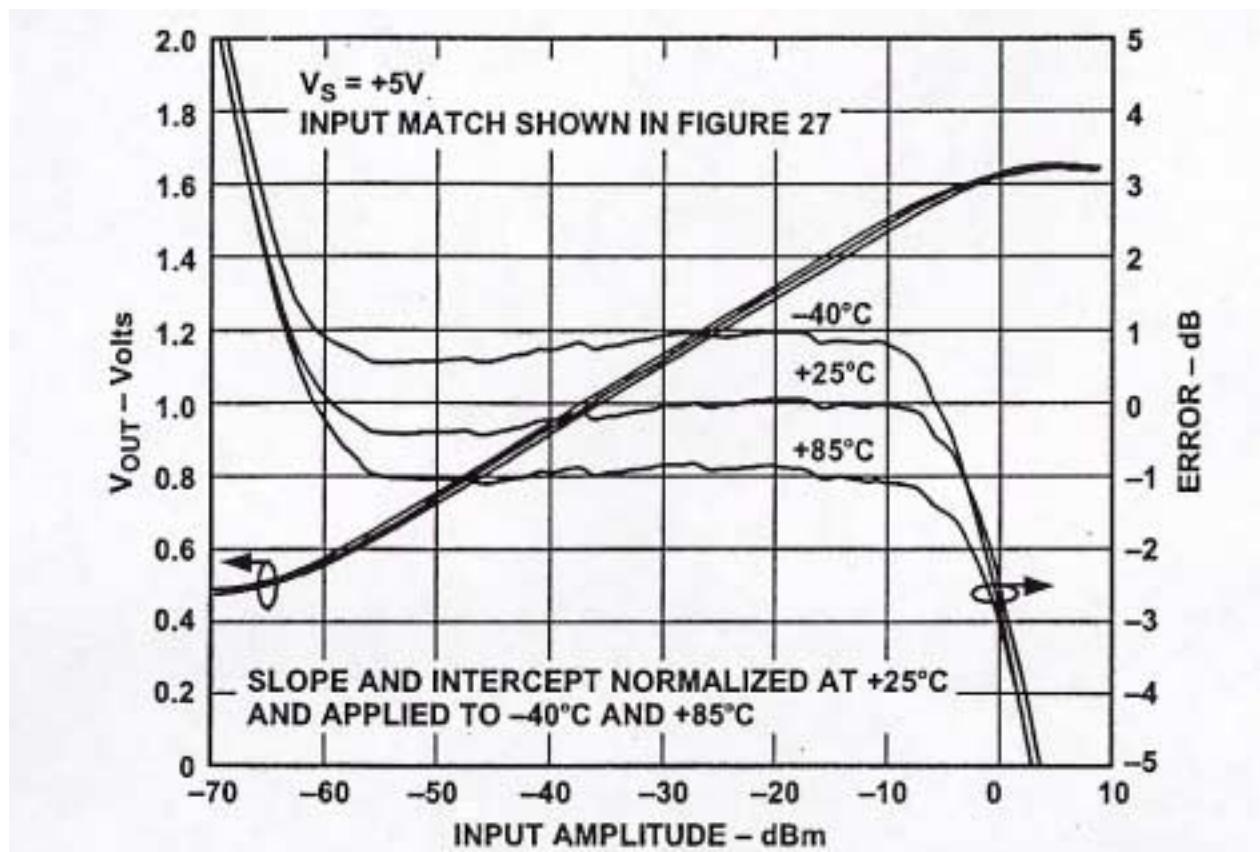


Figure 4.  $V_{OUT}$  and Log Conformance vs. Input Amplitude at 100 MHz;  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$

# AD8313 Response at 900 MHz

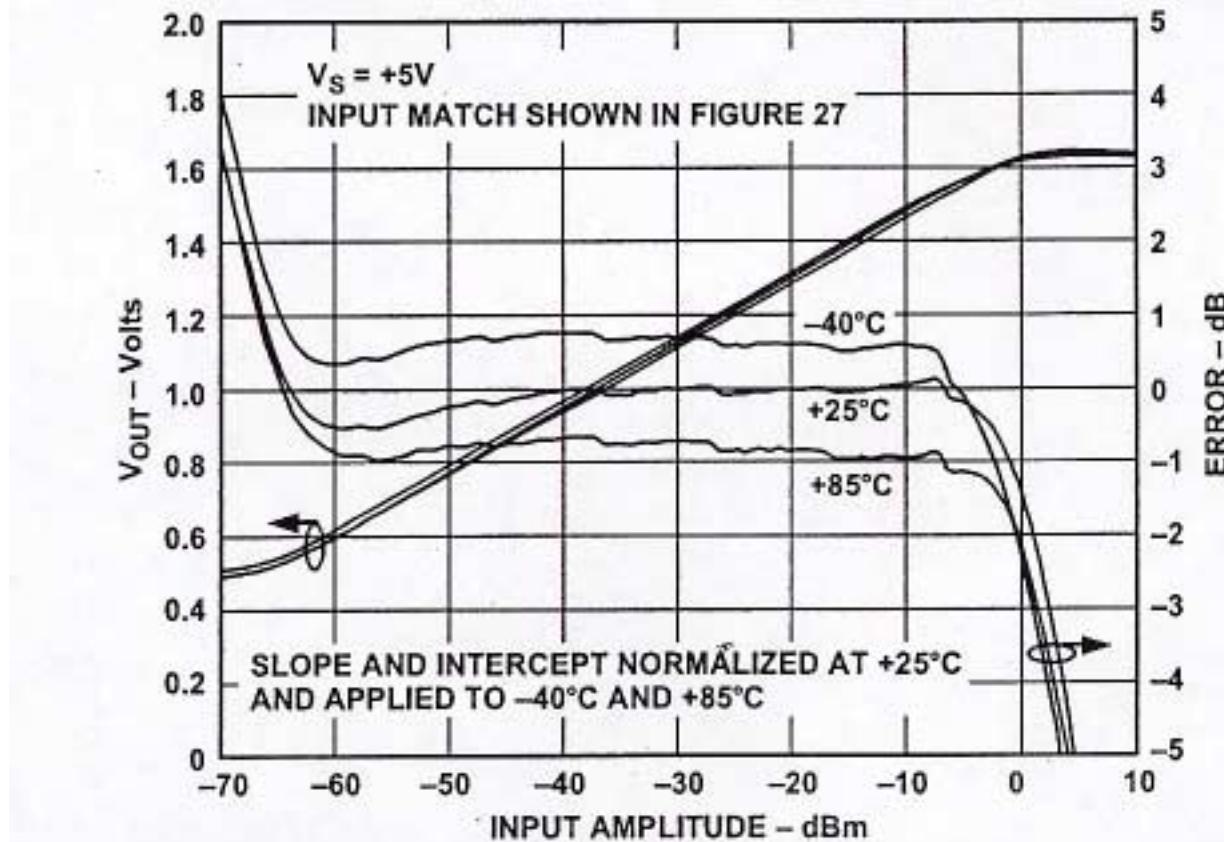


Figure 5.  $V_{OUT}$  and Log Conformance vs. Input Amplitude at 900 MHz;  $-40^{\circ}\text{C}$ ,  $+25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$

# AD8313 Video Risetime

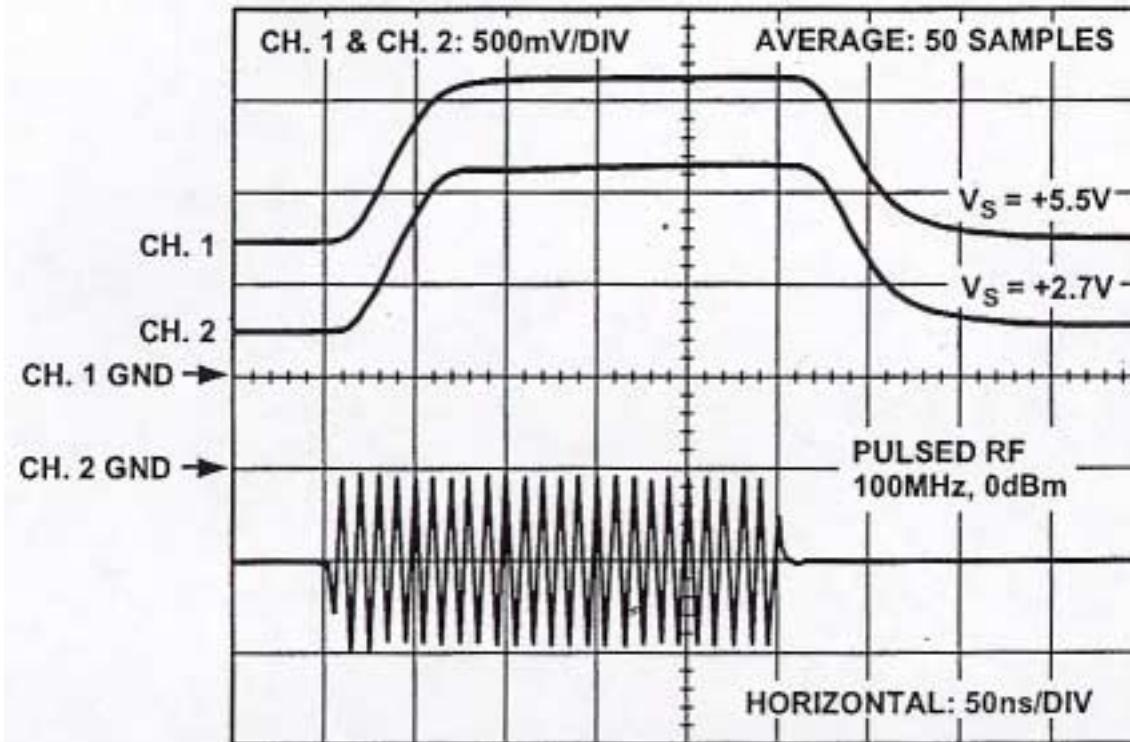
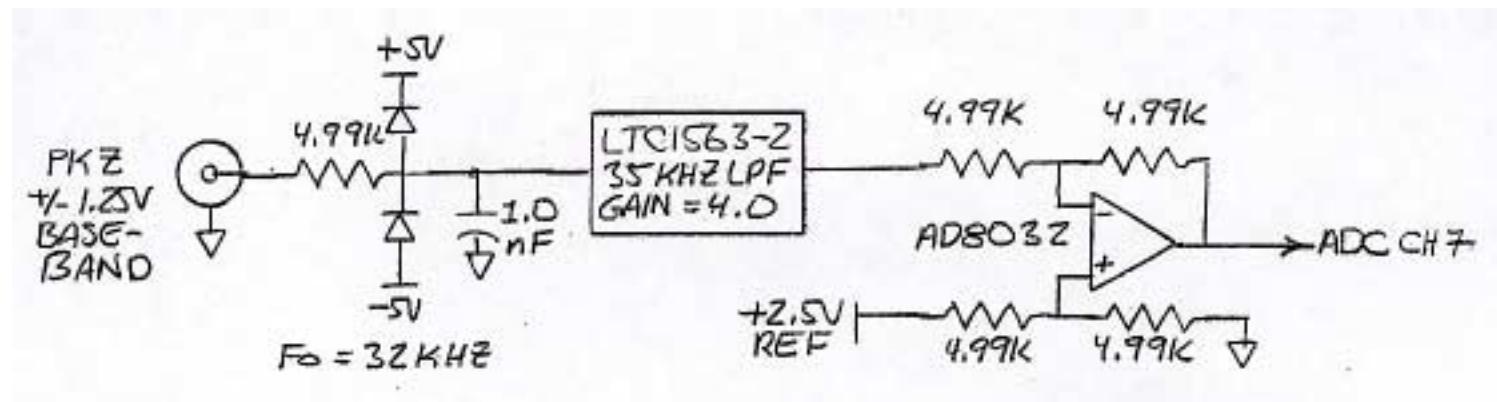


Figure 18. Response Time, No Signal to +0 dBm

# Baseband Front End



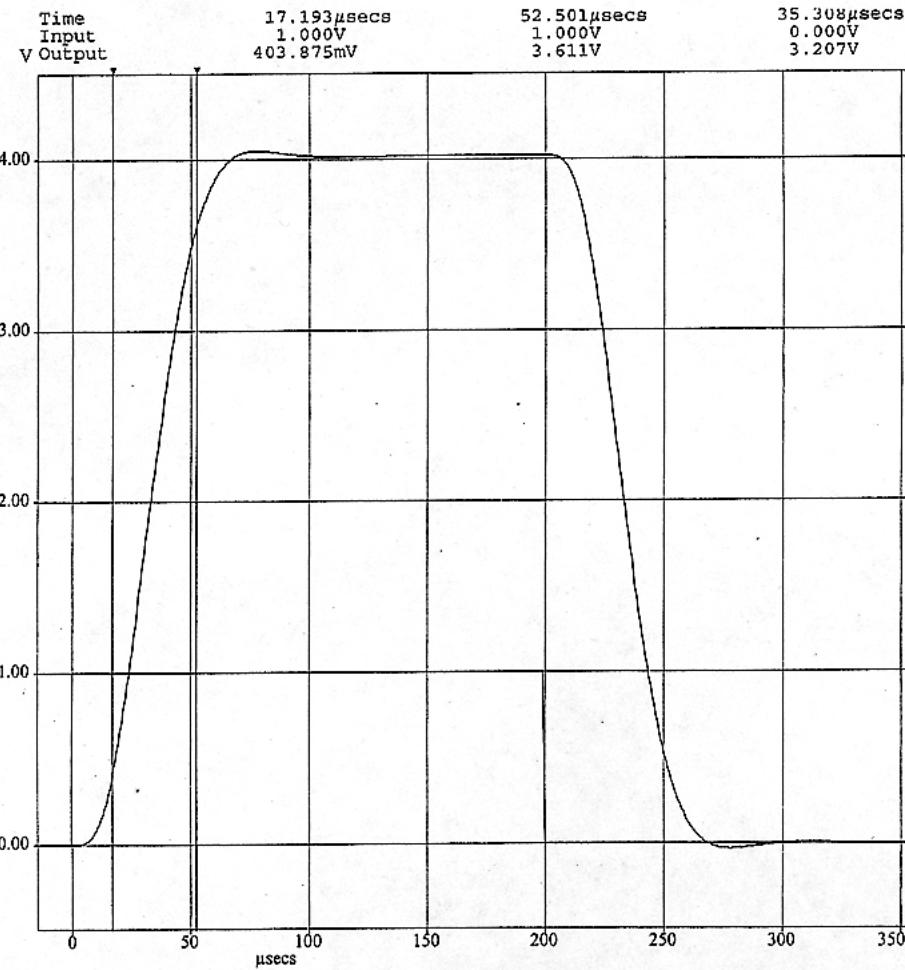
# 10 kHz Filter Impulse Response



SNS Bessel 4 Pole LPF

Title: SNS Bessel 4 Pole LPF  
Sign Specification  
Filter Response: Bessel  
Filter Type: Lowpass  
Order: 4

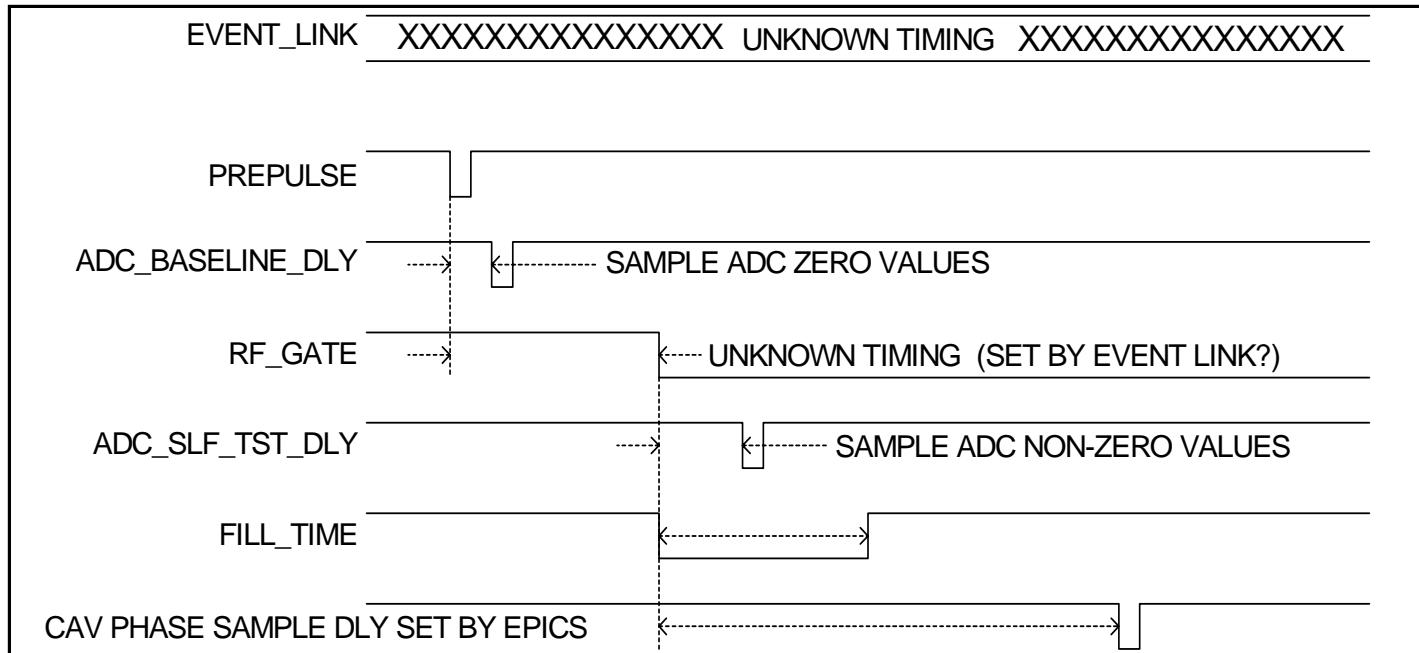
Passband Ripple: 0.000dB  
Stopband Attenuation: 22.700dB  
Passband Frequency: 10.000kHz  
Stopband Frequency: 40.000kHz



# Analog Accuracy Enhancements



- Baseline subtract for power detector offset correction.
- Stuck at zero fault detection by sampling during FILL\_TIME.



# VXIbus Interfaces



Channel	Name	Source	User	Function
ECLTRG00	40MHZ	CDM	ALL	40 MHZ clock (rising edge mark)
ECLTRG01	10MHZ	CDM	ALL	10 MHZ clock (rising edge mark sync'd to 40 MHz)
LBUS[00..11]	LBUS			Not used
TTLTRG0*	SAMPLE*	CDM	ALL	Synchronous data sample strobe. Latch data on falling edge, clear data registers on rising edge.
TTLTRG1*	SRF_INHIBIT	FRCM	HPM	SRF tuning mode fault inhibit. Orders HPM to ignore RF faults for duration of SRF_TIME during tuning of SRF cavities. Timer starts on falling edge of SRF_INHIBIT.
TTLTRG2*				Spare
TTLTRG3*	RF_GATE*	CDM	ALL	LOW when RF is ON / HIGH when OFF.
TTLTRG4*	T0	CDM	ALL	T0 sync pulse from master timing system. Falling edge is fiducial.
TTLTRG5*	FAULT_L*	ALL	HPM	RF fault in LEFT half of crate. (Klystron A). LOW = FAULT (RF off)
TTLTRG6*	RF_FAULT*	FRCM HPM	MPS	Tell MPS to turn off beam during faults. LOW = FAULT (Beam off)
TTLTRG7*	FAULT_R*	ALL	HPM	RF fault in RIGHT half of crate. (Klystron B). LOW = FAULT (RF off)

# Front Panel Built-In-Test



- LED Indicators stretched to 50 ms:

MODSEL	RF_GATE
RF_PERMIT	RF_FAULT
FOARC	HPM_FAULT
- Multiplexed test point to one front panel SMA:
  - All FOARC Inputs.
  - All analog feeds (detected RF) to ADC.
  - All TTLTRG\* backplane signals.
  - Channels selected *via* EPICS.

# Internal Built-In-Test

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- Internal power supply monitoring.
- Analog/ADC fault monitoring to detect stuck at zero and stuck at rail faults.
- FOARC “Lamp Test” function.
  - Possible “LED Test” function under consideration.
- Internal clock failure diagnostics (one-shots).
- Internal 40 MHz clock test oscillator independent of backplane clock signals.

# Mistake Proofing



- Part number G-level reflects application (channels and frequencies) and will be readable via EPICS.
- Module extractors will be color-coded by frequency.
- Installing a reduced-channel module (e.g.: a six-channel -G02 in a seven-channel –G03 slot) will be detected because the missing signal will show a “stuck at zero” fault.

# Design and Test



- Schematic capture and board layout by contractor. Interface to the CAE contractor is through the LANSCE-8 CAE shop.
- VXIbus interface uses proven Matt Stettler/LANL design. PLD logic design by Mark Prokop.
- Hardware functional test will exercise all inputs (analog and opto) and verify correct action.
- Calibrated signal generator used to set detector zero and span pots. Cal pots will be locked.
- G-level of each board will be set by EPICS-readable solder jumpers on each board.
- The contract manufacturing plan will be discussed by Irene DeBaca.

# Open Issues

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- Will the proposed cavity arc detection strategy work with SRF cavities? (Curt Hovater/Lloyd Young?)
- What is overall timing source and interface?
  - How is SAMPLE controlled?
- How deep do the history buffers need to be?
- When will we decide on two or three RFCS/crate?
- Do we need to support the FOARC LED test?

# Clock Module Overview

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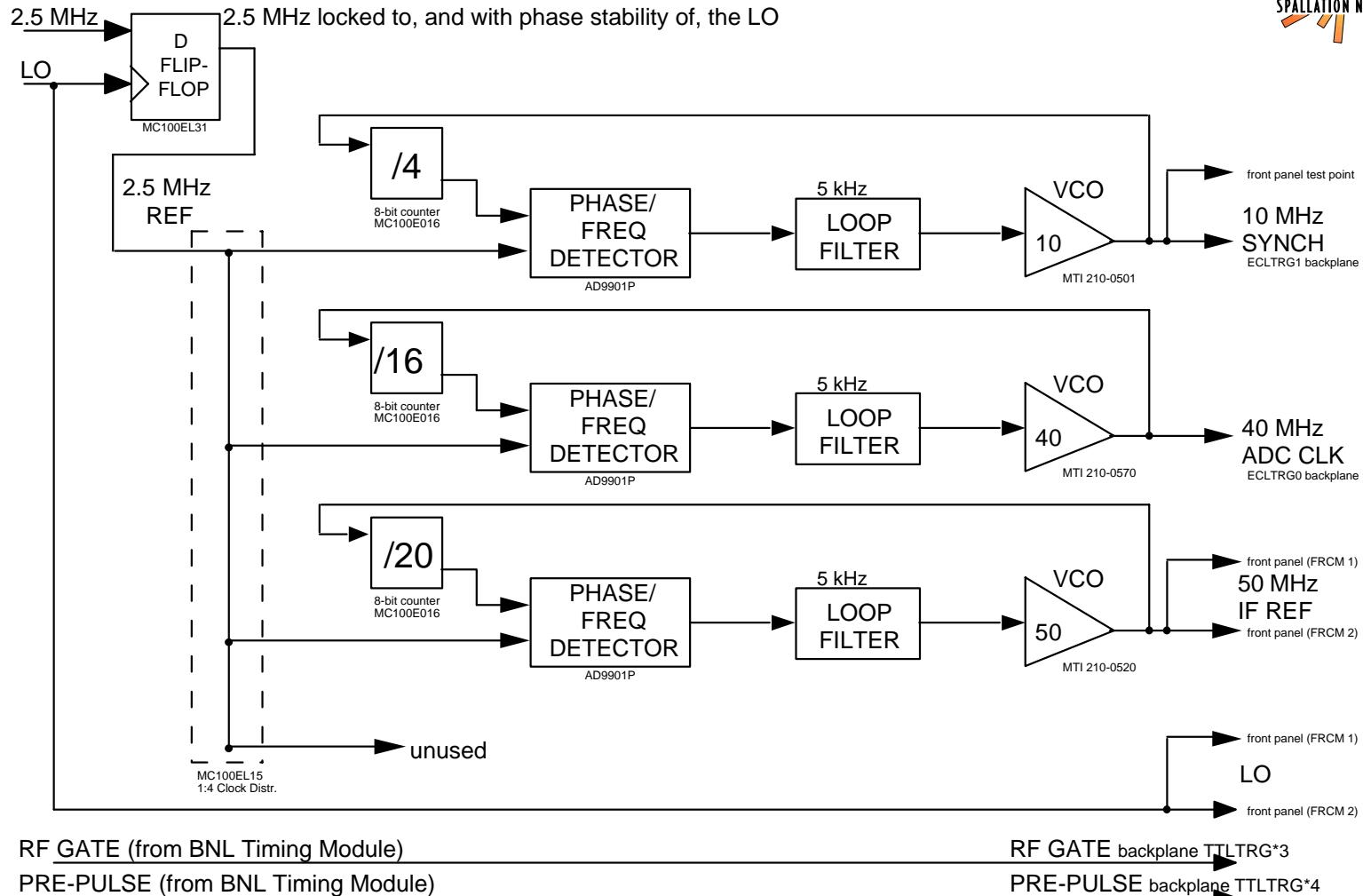
- REQUIREMENTS AND SPECIFICATIONS
- CDM WITHIN OVERALL RF CONTROL SYSTEM
- BLOCK DIAGRAM
- I/O REQUIREMENTS
- FAILURE/RESET MODES
  - BUILT IN SELF-TEST

# REQUIREMENTS & SPECIFICATIONS

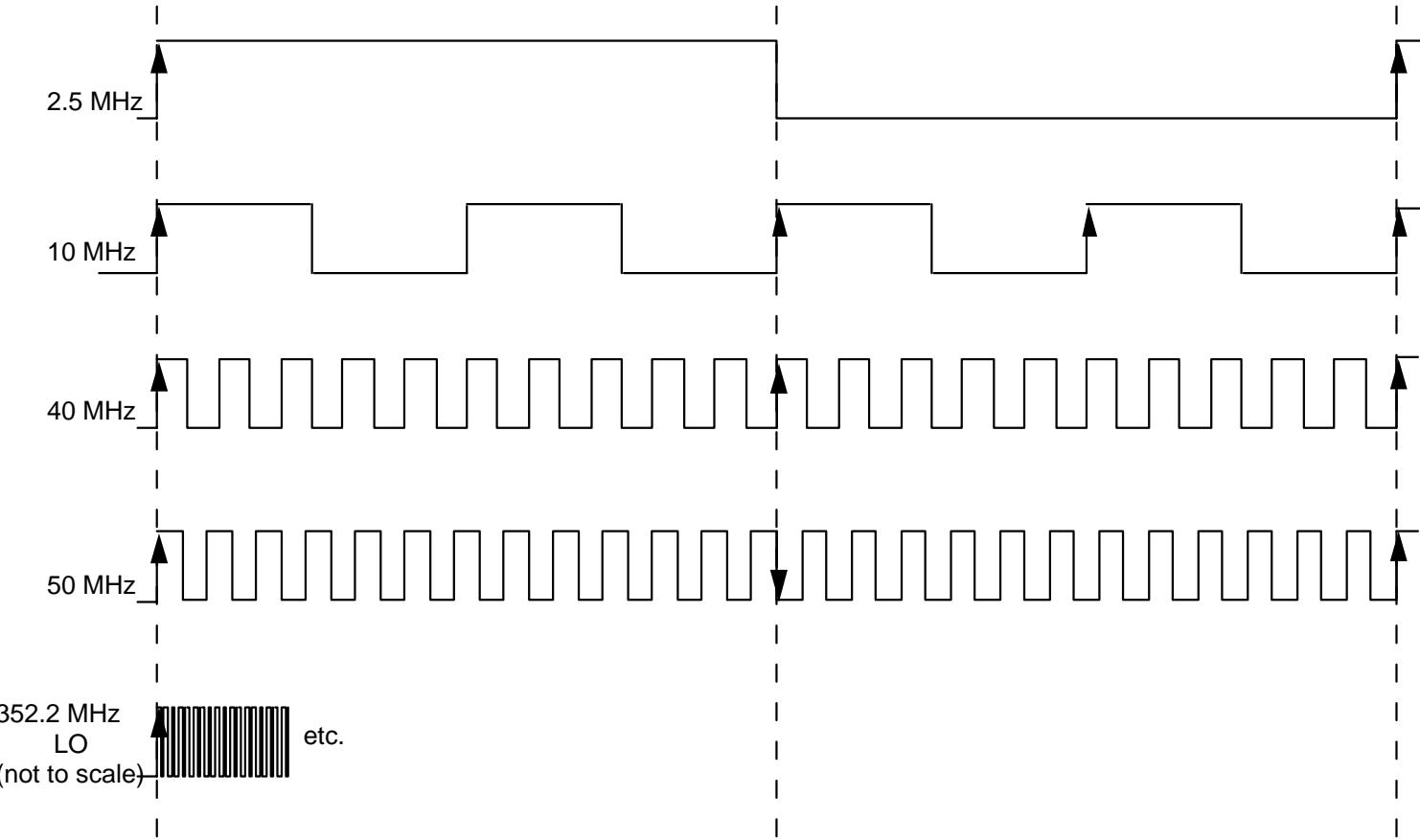


- PROVIDE SYNCHRONIZED CLOCKS TO ALL RF CONTROL MODULES.
  - ALL DERIVED FROM, & PHASE-LOCKED TO, THE MASTER OSCILLATOR
- PROVIDE INTERFACE BETWEEN TIMING MODULE AND ALL RF CONTROL MODULES
- PHASE-LOCKED OUTPUTS:
  - 40 MHz ADC CLOCK ( $\pm 0.1$  degree)
  - 50 MHz IF ( $\pm 0.1$  degree)
  - 352.5 (755) MHz LO ( $\pm 0.1$  degree)
- OTHER OUTPUTS (backplane)
  - SYNCHRONIZATION PULSE (10 MHz); RF GATE; SAMPLE
- INPUTS
  - 2.5 MHz REFERENCE
  - LO (temperature compensated)
  - TIMING (front panel)

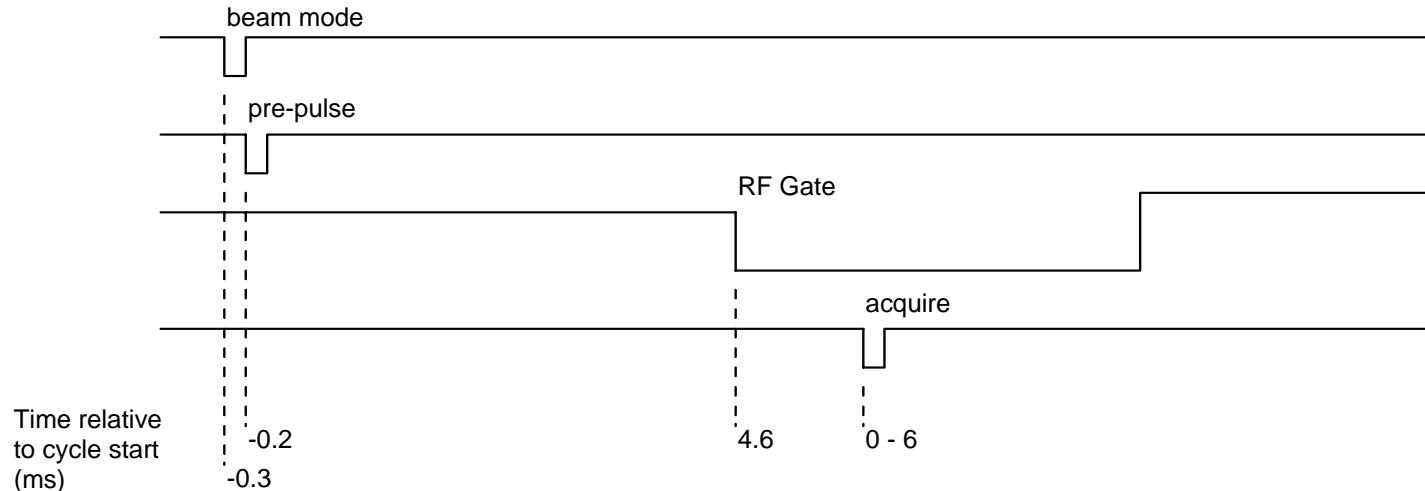
# Clock Module Phase-Locked Loop Implementation



# Clock Module Timing Relationships



# EXTERNAL TIMING SIGNALS



**beam mode:**

IOC is interrupted on the RTDL valid event and immediately writes the "beam mode" frame to registers on the FRCM modules

**pre-pulse:**

indicated that all required parameters have been written to the RF modules. TTL signal on VXI trigger bus

**RF Gate:**

triggers predetermined RF cycle. Precedes beam by 400 turns. This number of turns can optionally be adjusted to make the pulse precede beam by a fixed time, independent of event link period. TTL signal on VXI trigger bus

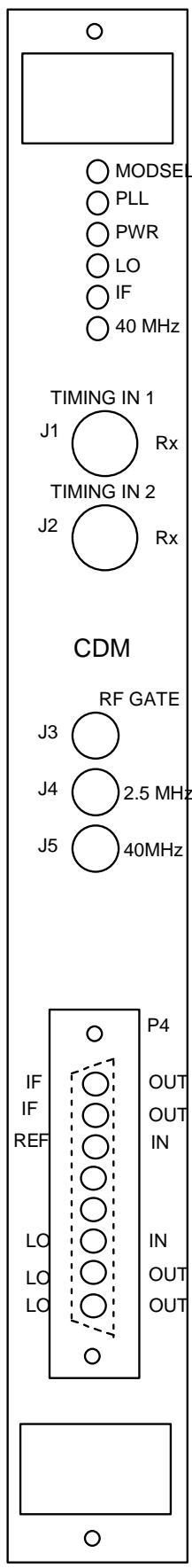
**acquire:**

triggers the acquisition of data for diagnostic purposes. TTL signal on VXI trigger bus

**Cycle Start**

Resets fault counters, starts delay counters, gate delay counters, etc. Systems with fine timestamp requirements start counting 16 MHz carrier cycles from this event.

# Clock Module Front Panel

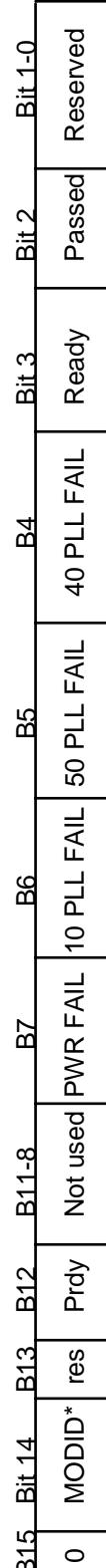


# CDM VXIbus ADDRESS MAP



## A16 ADDRESS SPACE:

OFFSET	REGISTER NAME	VALUE
00 <sub>16</sub>	LANL MANUFACTURER'S ID	7FA0 <sub>16</sub>
02 <sub>16</sub>	DEVICE TYPE	FF4B <sub>16</sub>
04 <sub>16</sub>	STATUS/CONTROL	XXXX <sub>16</sub> see below
06 <sub>16</sub>	OFFSET	0000 <sub>16</sub>
08 <sub>16</sub>	ATTRIBUTE	XXX7 <sub>16</sub>
0A <sub>16</sub>	SERIAL NUMBER LOW	000X <sub>16</sub>
0C <sub>16</sub>	SERIAL NUMBER HIGH	0000 <sub>16</sub>
0E <sub>16</sub>	VERSION NUMBER	0000 <sub>16</sub>
10 <sub>16</sub>		BAD <sub>16</sub>
12 <sub>16</sub>		BAD <sub>16</sub>
14 <sub>16</sub>		BAD <sub>16</sub>
16 <sub>16</sub>		BAD <sub>16</sub>
18 <sub>18</sub>		BAD <sub>16</sub>
1A <sub>16</sub>		BAD <sub>16</sub>
1C <sub>16</sub>		BAD <sub>16</sub>
1E <sub>16</sub>		BAD <sub>16</sub>
20 <sub>16</sub>		BAD <sub>16</sub>
22 <sub>16</sub>		BAD <sub>16</sub>
24 <sub>16</sub>		BAD <sub>16</sub>
26 <sub>16</sub>		BAD <sub>16</sub>
28 <sub>16</sub>		BAD <sub>16</sub>
2A <sub>16</sub>		BAD <sub>16</sub>
2C <sub>16</sub>		BAD <sub>16</sub>
2E <sub>16</sub>		BAD <sub>16</sub>
30 <sub>16</sub>		BAD <sub>16</sub>
32 <sub>16</sub>		BAD <sub>16</sub>
34 <sub>16</sub>		BAD <sub>16s</sub>
38 <sub>16</sub>		BAD <sub>16</sub>
3A <sub>16</sub>		BAD <sub>16</sub>
3C <sub>16</sub>		BAD <sub>16</sub>
3E <sub>16</sub>		BAD <sub>16</sub>



# TEST ITEMS

---



## Built In Test

- LEDs
- Loop Lock Indicators
  - Backplane Power Fail
  - Loss of Timing Indicators
  - Power Out Indicator

Control Status Register – Echo Information to EPICS

F. P. Test Points – Loops, Timing

Module Test Philosophy

put in inputs, measure outputs

# CDM STATUS/SUMMARY



- MODULE WILL PROVIDE SYNCHRONIZED CLOCKS
- 40, 50 MHz LOOPS HAVE BEEN BREADBOARDED
- FAULT CIRCUITRY BUILT AND TESTED
- STILL NEED TO TEST STABILITY OF LOCKING THE 2.5 MHz TO THE STABLE LO
- TIMING CIRCUITRY COPIED FROM RHIC - SHOULD WORK FIRST TIME
- SCHEMATICS ARE INTO ECAD
- WHAT HAVE I MISSED?

# LLRF Global Control System

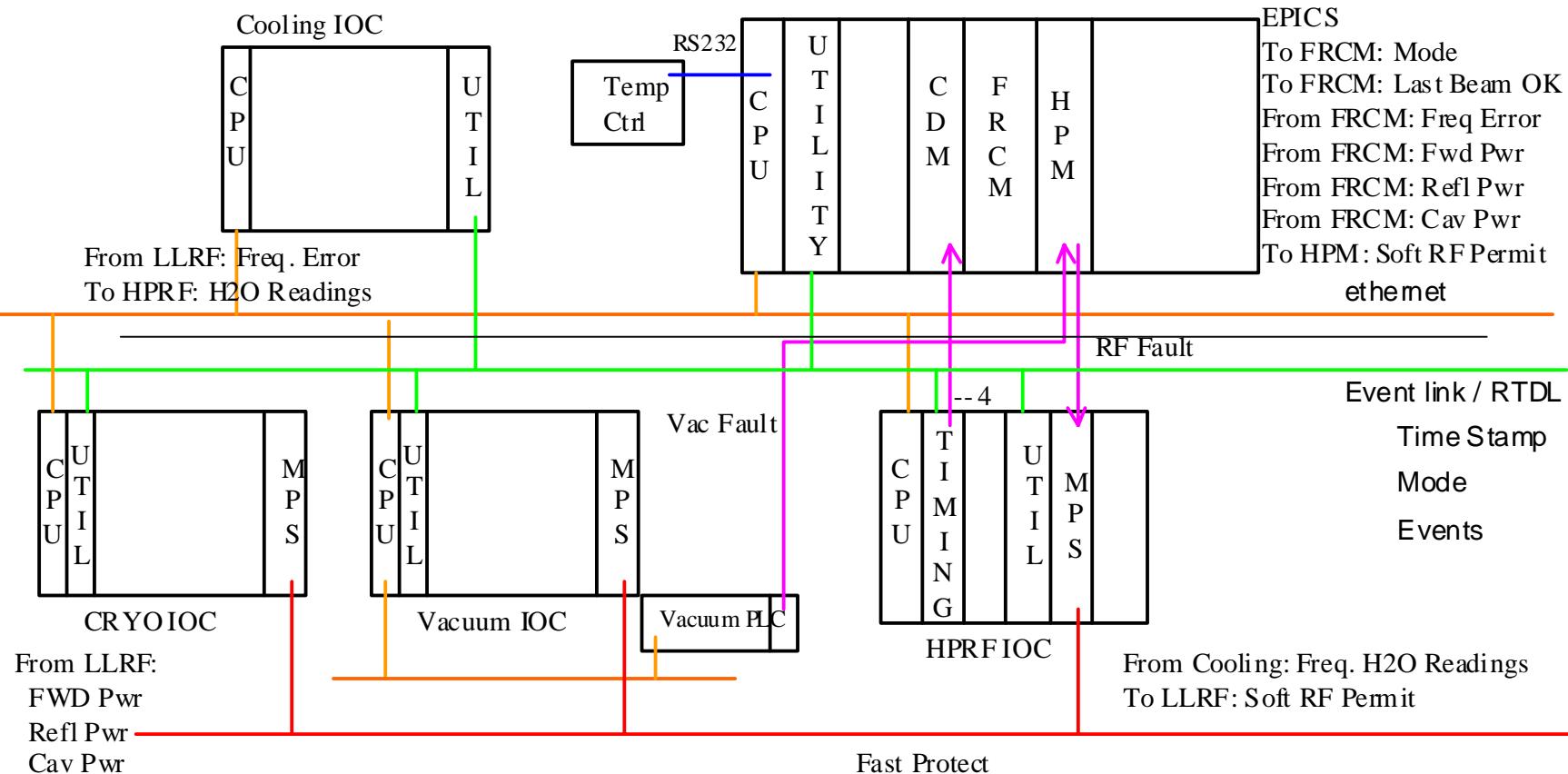


Deb Kerstiens

SNS-4

16 January 2001

# LLRF Global Control System Interfaces

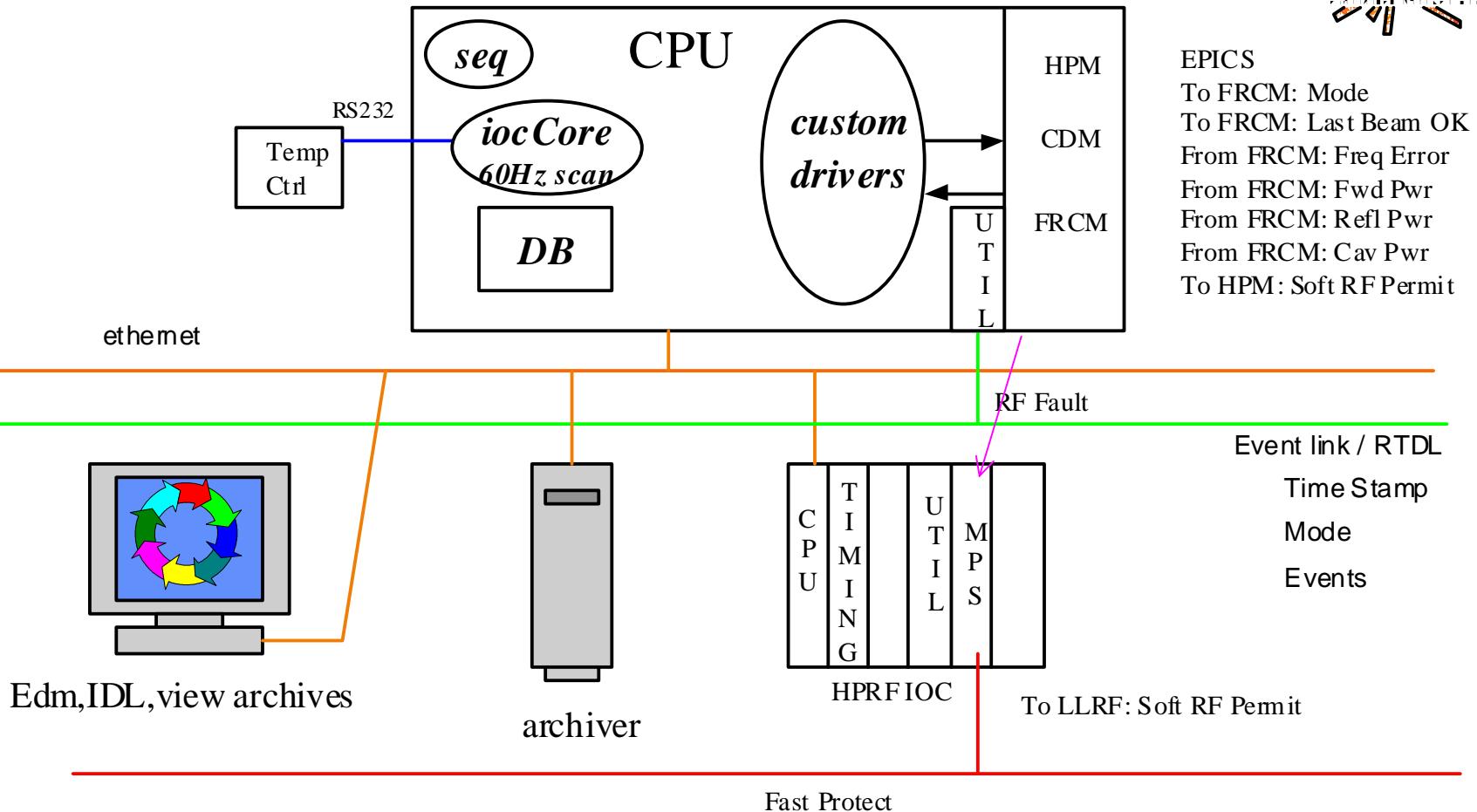


# LLRF IOC and Operator Interface



- IOC will be a Heurikon baja60 processor
- IOC software will include:
  - EPICS 3.14.x (iocCore, record, device, driver support)
  - 60Hz scan rate for database processing
  - EPICS sequencer
  - custom device and driver support for LLRF modules
- Operator interface tools will include:
  - edm (for control and status)
  - stripTool, alarm handler
  - archiver, save and restore tool
  - data visualization tools (IDL, ?)
  - other tools (ELOG, etc.)

# LLRF IOC and OPI Software

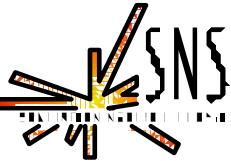


# LLRF Global Controls Development



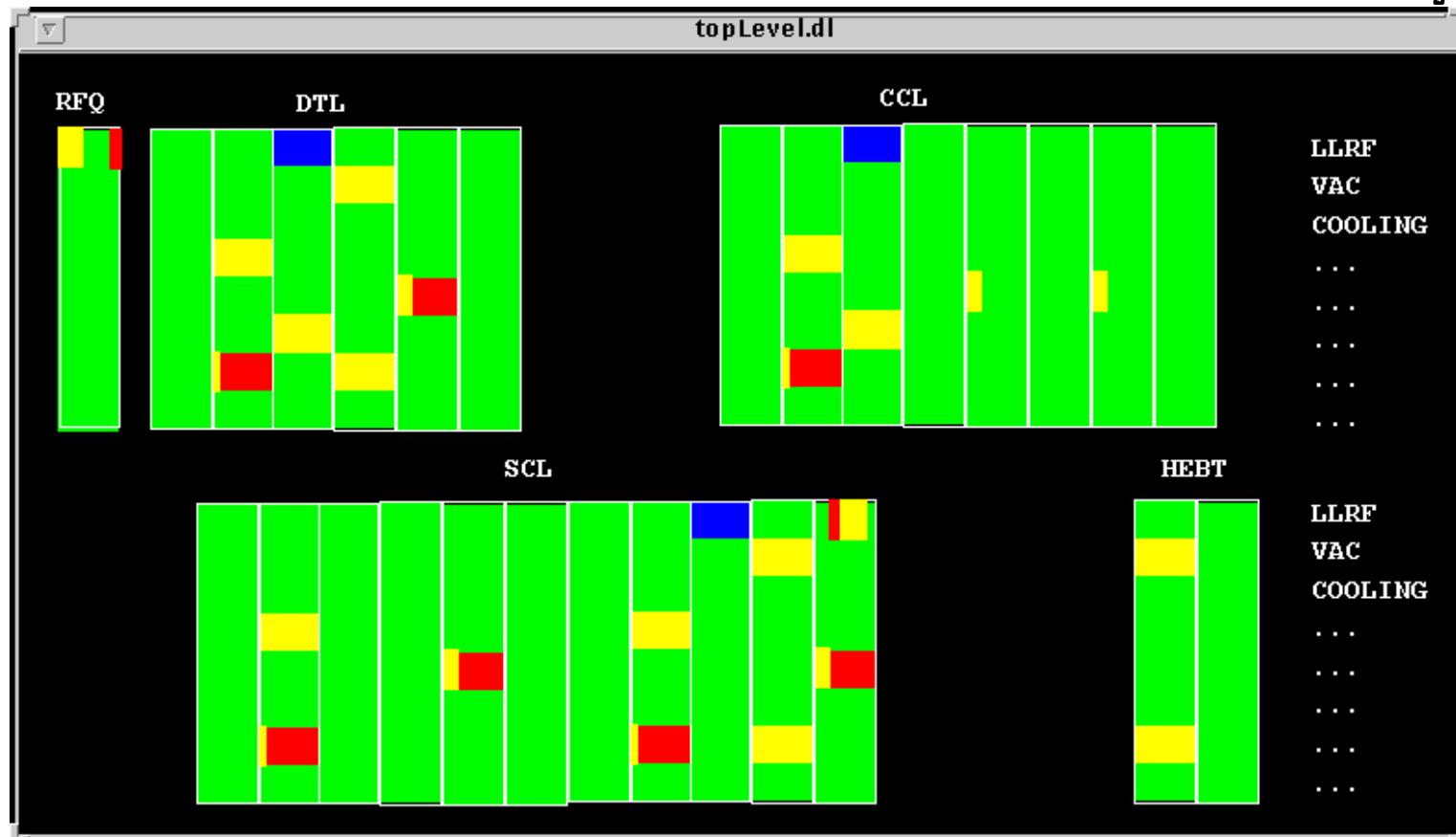
- LLRF software will be developed in the SNS standard development environment :
  - EPICS
  - LINUX
  - ORACLE
  - CVS
- Initial definition of LLRF modules provides initial requirements
  - testing
  - prototyping
- LLRF functionality provides high level requirements

# LLRF Global Controls Issues



- Date sampling rate for viewing is 300 points at 2 Hz
  - Archiving 32K of 32 bit data at 60 Hz would require a change in EPICS Channel Access--do we need this?
- Interface definition with RTDL, Event Link, Timing, and MPS issues is still a bit “rough”
- Software requirements follow module design and testing
- LLRF global controls will support
  - engineering
  - commissioning and operation
- Data visualization software is required but not defined
  - selected by SNS? (if so, when?)
- Other issues?

# Global Controls Top Level Display



# Global Controls LLRF Display



llrf\_top.dl

### Low Level RF Controls

HPM Latch Arc RFQ HP CB RF Trip (ACM)  
Arc Lat Arc Lat Lat RF Trip (HPM) RFQ Arc

Hi (kHz) Deadband Frequency  
Inner Outer  
< > 5.00 < > 15.00  
< > 5.00 < > 15.00

Low (kHz)

Digital Loop Feedback Integrator  
Analog Loop Feedback

Open OPEN OPEN

Freq Offset (kHz) Amplitude (0-100%) Digital Analog Open Loop  
< > 15.00 < > 51.50 < > 62.00 < > 34.00  
-0.00 < > 0.00 < > 0.00 < > 0.00

Operating Mode

Pulse Width(ms) Rep Rate(ms) Maximum(0-100%) Minimum(0-100%)  
< > 1.90 < > 2.00 < > 51.00 < > 9.00

Duty Factor (%) Mode CW I/Q (Amp/Ph) Set Mode Exit

# Cost



- RF Controls Overall cost through integration: \$15.4M
  - includes NC system, SRF system (92 cavities), Reference system.
  - “Integration” ⇒ hooking up to various external systems and testing.
  - (Commissioning with beam is included in a different work package)
- Philosophy:
  - Build first few systems at LANL to prove out design, then go out to Industry for Manufacture of Modules as well as Test
  - Integrate first systems with EPICS at LANL, then install and integrate at ORNL. LANL personnel heavily involved up front but rapidly taper to “consulting” role

# Near-Term Schedule



- Module Design 7/1/00 - 4/1/01
    - PDR
    - Schematics “Board Design & Layout” 9/1/00 - 7/1/01
    - 1,2 PCB’s
    - FDR
    - Documentation
  - Vendor Selection 12/1/00 - 2/1/01; 3/1-6/13/00
  - Build & Test 2-4 7/1/01 - 9/1/01
  - Build / Test 5-16 (Contract Manufacturer) 9/01 - 1/02
  - Integration in lab: first system 6/13 - 8/21/01

# Integration & Commissioning Plan



## First system of each type (NC 402.5 MHz, NC 805 MHz, SRF 805 MHz)

MHz)

- Test complete system with EPICS at LANL
- Provide oversight for cable installation and rack installation at ORNL
- Ship to ORNL
- Install / Integrate with external systems in situ, with ORNL support

## Next 2-4 systems of each type

- Ship directly to ORNL from Contract Manufacturer
- Install / Integrate with external systems in situ, with ORNL support

## 5-N systems

- Support ORNL installation integration efforts

# Integration & Commissioning Issues



- Identifying correct ORNL personnel early enough to get them properly trained
- Insuring requirement “creep” does not occur, without proper schedule and budget compensation
- Completing full documentation for system hand-off

# Technical Issues - External system interfaces a manageable concern.



## Top Level System-wide External Interfaces for RFCS

- Timing ( $T_0$ , modes of operation);
  - Cavity Resonance Control System ( $f_{res}$  error);
  - HPRF forward/reflected power directional couplers, fiber optic arc detectors;
  - Machine Protect System
    - Fast Protect (turn beam off);
    - RF Permit (RF-on OK) - includes Vacuum Permit, Cryomodule Interfaces;
  - Cavity pickup loops (field instrumentation);
  - Beam Diagnostics (Beam feedforward);
  - EPICS
- Multi-lab communication has improved. Video conferences quite useful.
  - EPICS personnel involved in RF Control design meetings.

# RF Controls Summary



- **System specification released; available on the web**
- **Module designs progressing**
  - Have bread-board key components
  - Schematics into ECAD for Printed Circuit Board Layout now
- **Reference line prototype pieces have been ordered**
  - mockup to be built and tested February 2001 - delay in parts shipment till then

# REMAINING ISSUES?

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- SHIELDED RACKS - necessary or not?